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# HannStar Product Information

MODEL : **HSD150SX82**

**-X**

ISSUE DATE: 2001-05-18

- Note :
1. The information contained herein is tentative and may be changed without prior notices.
  2. Please contact HannStar Display Corp. before designing your product based on this module specification.
  3. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by HannStar for any intellectual property claims or other problems that may result from application based on the module described herein.



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### Record of Revisions



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## 1.0 GENERAL DESCRIPTION

### 1.1 Introduction

HannStar Display model **HSD150SX82** is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, the voltage reference, common voltage, column, and row driver circuit. This TFT LCD has a 15-inch diagonally measured active display area with XGA resolution (768 vertical by 1024 horizontal pixel array).

### 1.2 Features

- 15" XGA TFT LCD panel
- 2 CCFLs Backlight system
- Supported XGA (V:768 lines, H:1024 pixels) resolution
- Supported to 75Hz refresh rate
- Without LCD Timing Controller

### 1.3 General information

Item	Specification	Unit
Outline dimension	<b>340 x 250.1 x (14.3) (max.)</b>	mm
Display area	304.1(H) x 228.1(V) (15.0" diagonal)	mm
Number of Pixel	1024(H) x 768(V)	pixels
Pixel pitch	0.297(H) x 0.297(V)	mm
Pixel arrangement	RGB Vertical stripe	
Display color	6-bits driver	
Display mode	Normally white	
Surface treatment	Antiglare, Hard-Coating(3H)	
Weight	<b>TBD (max.)</b>	g
Back-light	2-CCFLs, Bottom edge side	
Input signal	Source and Gate Driver control signals	
Power consumption	TBD	W
Optimum viewing direction	6 o'clock	

### 1.4 Applications

- Desktop monitors
- Moniputers
- Display terminals for AV applications
- Monitors for industrial applications

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### 1.5 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	--	<b>340</b>	--	mm
	Vertical(V)	--	<b>250.1</b>	--	mm
	Depth(D)	--	<b>13.8</b>	<b>14.3</b>	mm
Weight (without inverter)		--	<b>TBD</b>	<b>TBD</b>	

## 2.0 ABSOLUTE MAXIMUM RATING of TFT LCD Module

### 2.1 Absolute Rating of Environment

Item	Symbol	Min.	Max.	Unit	Note
Storage temperature	T <sub>STG</sub>	-20	65	°C	
Operating temperature	T <sub>OPR</sub>	0	50	°C	
Vibration(non-operating)	V <sub>NOP</sub>	--	1.5	G	(1)
Shock(non-operating)	S <sub>NOP</sub>	--	70	G	(2)
Storage humidity	H <sub>STG</sub>	10	90	%RH	(3)
Operating humidity	H <sub>OP</sub>	10	80	%RH	(3)
Low pressure(operating)	P <sub>LOP</sub>	697	--	HPa	(4)
Low pressure(non-operating)	P <sub>LNOP</sub>	116	--	HPa	(5)

Note (1) 5-500Hz sine wave, X, Y, Z each directions, 30 min/cycle.

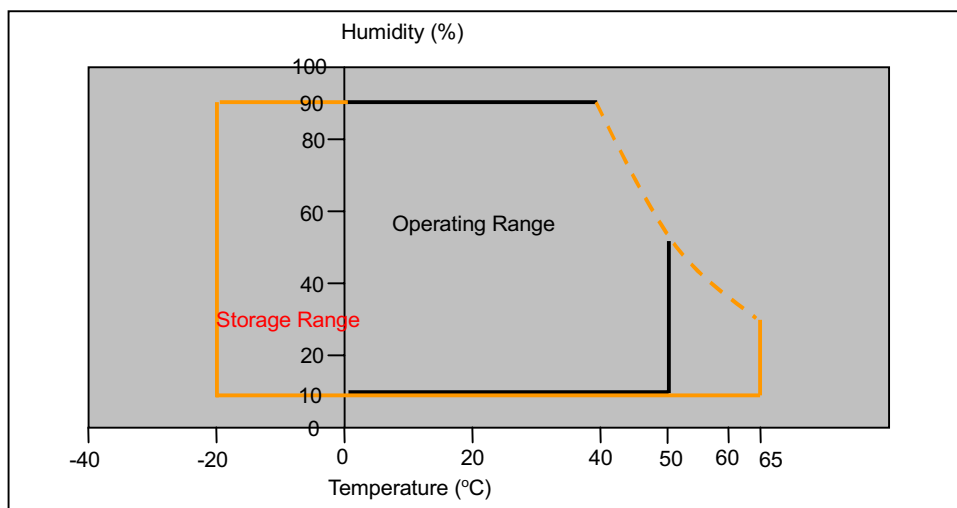
(2) 11ms, ±X, ±Y, ±Z direction, one time each. For this shock test, it is necessary to fill the silicon rubber between the shock jig as buffer.

(3) Max wet bulb temp. = 39°C

(4) 2hrs. (10000 feet)

(5) 24hrs. (50000 feet)

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## 2.2 Electrical Absolute Rating

### 2.2.1 TFT LCD Module

Item	Symbol	Condition	Value		Unit
			min.	max.	
Input Power Voltage	$V_{DD1}$	—	+2.8	+3.8	V(DC)
	$V_{GH}$		+20	+25	
	$V_{DD2}$		+8.0	+9.7	
	$V_{GC}$		-15.0	-12.0	
	$V_{GL}$		-7.0	-5.0	
Logic Signal input voltage	$V_{SIG}$	—	-0.3	$V_{DD1} + 0.3$	V

### 2.2.2 Back Light Unit:

Item	Symbol	Min.	Max.	Unit	Note
Lamp voltage	$V_L$	0	2000	V(rms)	(1)
Lamp current	$I_L$	—	7.0	mA	(1)
Lamp frequency	$f_L$	0	100	KHz	(1)

Note: (1) Permanent damage may occur to the LCD module if beyond this specification.

Functional operation should be restricted to the conditions described under Normal Operating Conditions.

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### 3.0 OPTICAL CHARACTERISTICS

#### 3.1 Measuring Condition

- Measuring surrounding : dark room
- Lamp current  $I_{BL}$  : **(6.0)**±0.1mA
- $V_{DD1}$ =3.3V,  $f_V$ =60Hz,  $f_{DCLK}$ =32.5MHz
- Surrounding temperature : 25±2°C
- 30min. Warm-up time.

#### 3.2 Measuring Equipment

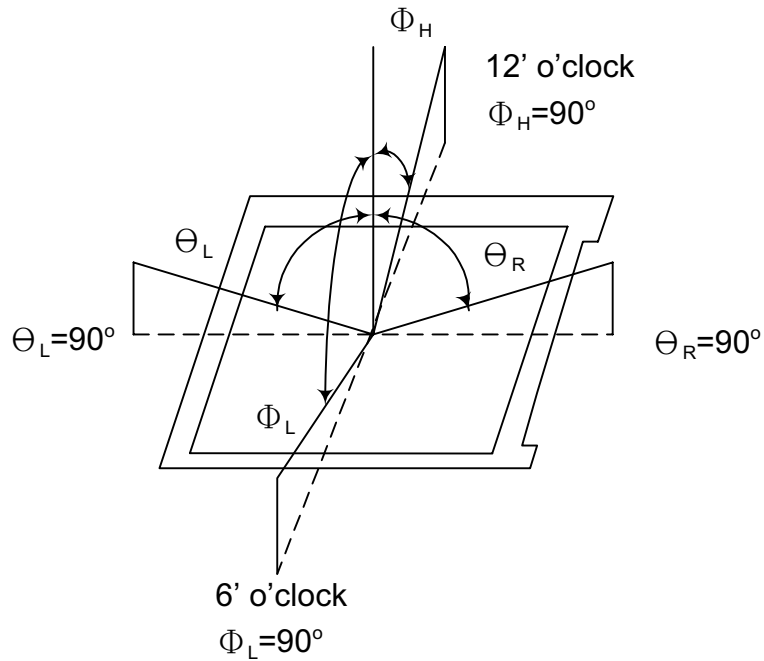
- LCD-7000 of Otsuka Electrics Corp., which utilized MCPD-7000 for Chromaticity and BM-5A for other optical characteristics.
- Measuring spot size : 10~12mm

#### 3.3 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast		CR		--	300	--		(1)(2)
Response time	Rising	$T_R$	$\theta=0^\circ$ $\phi=0^\circ$ Normal viewing angle	--	<b>(15)</b>	--	msec	(1)(3)
	Falling	$T_F$		--	<b>(35)</b>	--		
White luminance (center of screen)		$Y_L$		--	<b>(200)</b>	--	cd/m <sup>2</sup>	(1)(4)
Color Chromaticity (CIE1931)	Red	$R_x$	$\theta=0^\circ$ $\phi=0^\circ$ Normal viewing angle	0.57	0.62	0.67		(1)(4)
		$R_y$		0.28	0.33	0.38		
	Green	$G_x$		0.24	0.29	0.34		
		$G_y$		0.54	0.59	0.64		
	Blue	$B_x$		0.09	0.14	0.19		
		$B_y$		0.06	0.11	0.16		
	White	$W_x$		0.25	0.30	0.35		
		$W_y$		0.28	0.33	0.38		
Viewing angle	Hor.	$\theta_L$	CR>10	--	60	--		
		$\theta_R$		--	60	--		
	Ver.	$\theta_H$		--	40	--		
		$\theta_L$		--	<b>50</b>	--		
Brightness uniformity		$B_{UNI}$	$\theta=0^\circ$	60	--	--	%	(5)
Crosstalk		CT(n)	$\phi=0^\circ$	--	--	1.3	%	(6)

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Note (1) Definition of Viewing Angle:

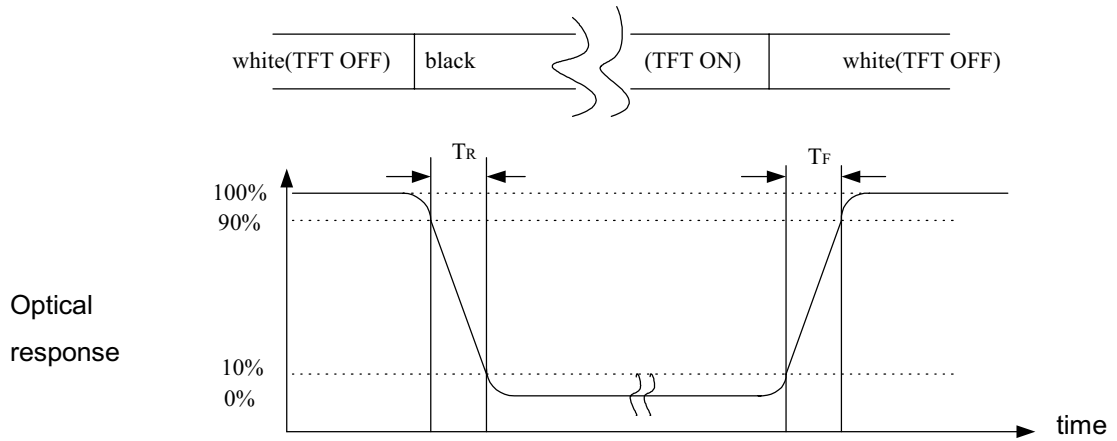


Note (2) Definition of Contrast Ratio(CR) :  
 measured at the center point of panel

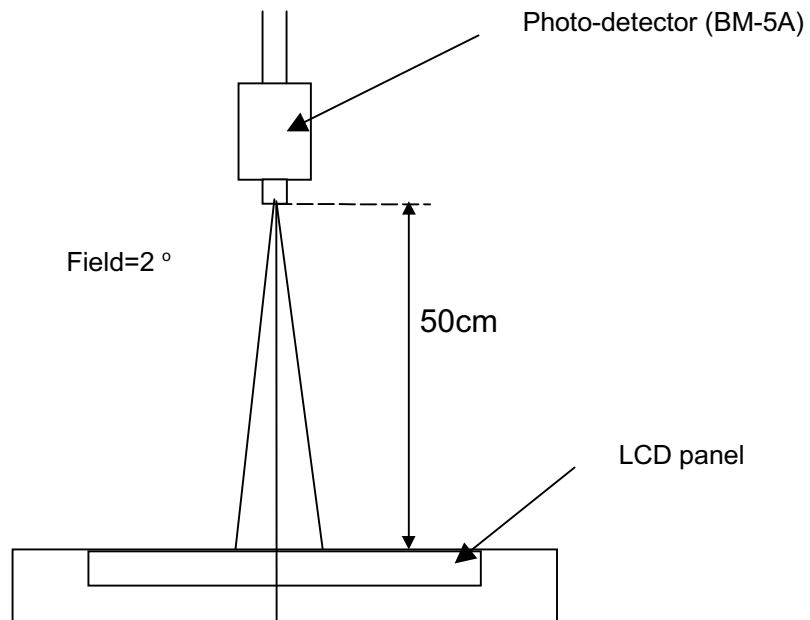
$$CR = \frac{\text{Luminance with all pixels white (L63)}}{\text{Luminance with all pixels black (L0)}}$$

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Note (3) Definition of Response Time: Sum of  $T_R$  and  $T_F$



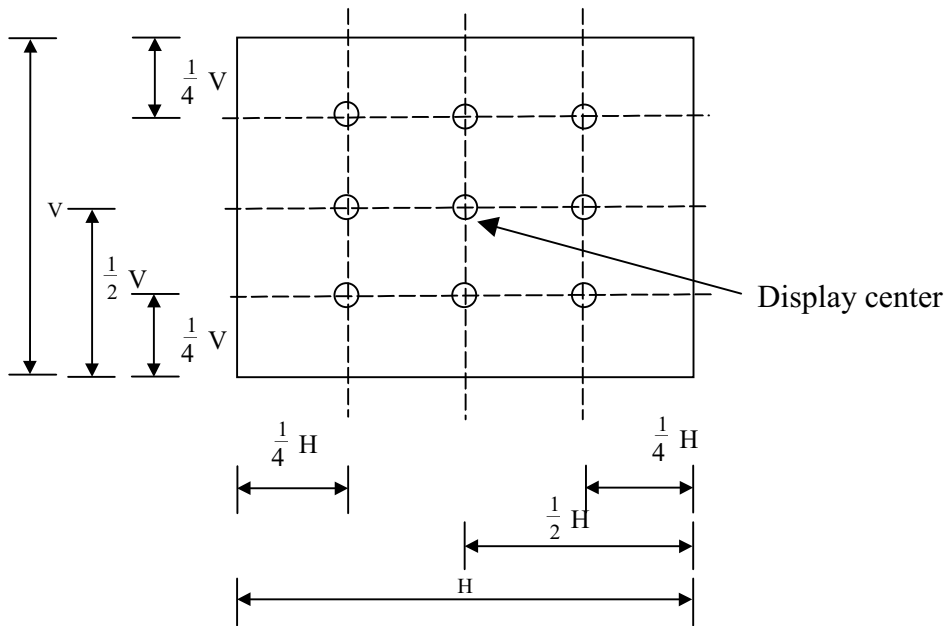
Note (4) Optical characteristic measurement setup



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Note (5) Definition of brightness uniformity

Luminance uniformity = (Min Luminance)/(Max Luminance) x 100%



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Note (6) Definition of crosstalk CT(1) ~ CT(4)

$$CT(n) = \frac{|L(n) - LB(n)|}{L(n)} \times 100\% , n = 1 \sim 4$$

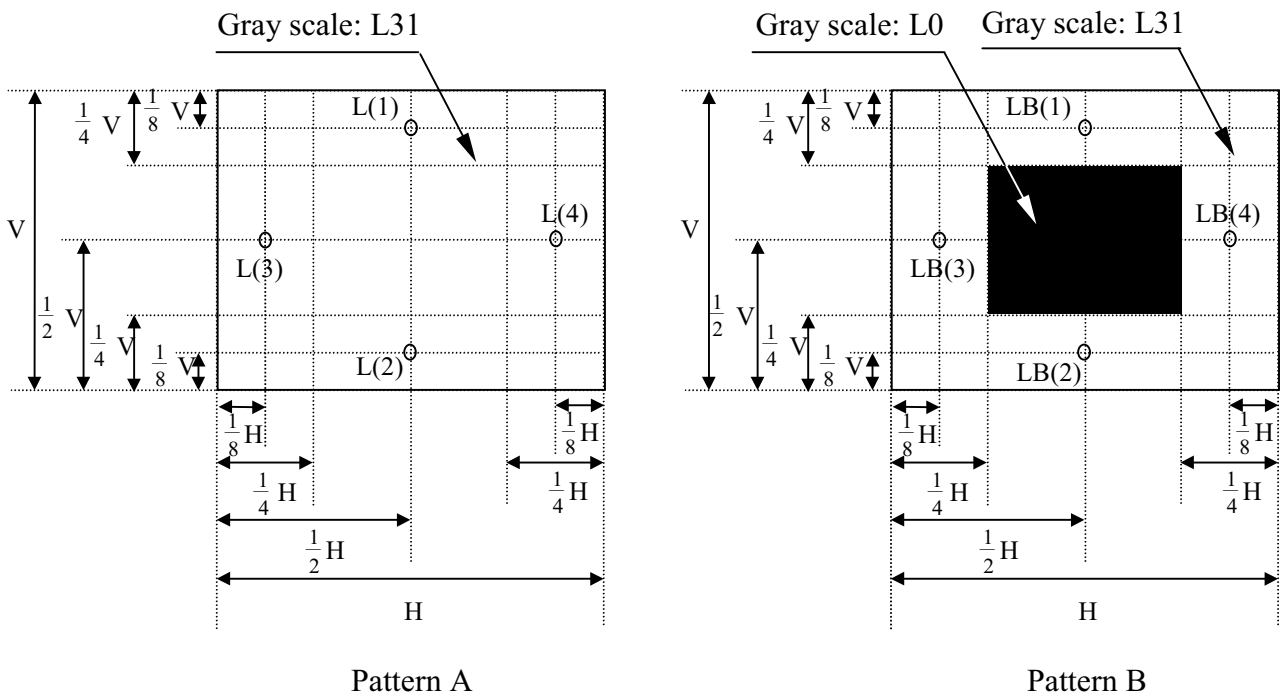
Where L(n) = Luminance of point "n" at pattern A (cd/m<sup>2</sup>) , n=1~4

LB(n) = Luminance of point "n" at pattern B (cd/m<sup>2</sup>) , n=1~4

The location measured will be exactly the same in both patterns.

L0 : Luminance with all pixels black

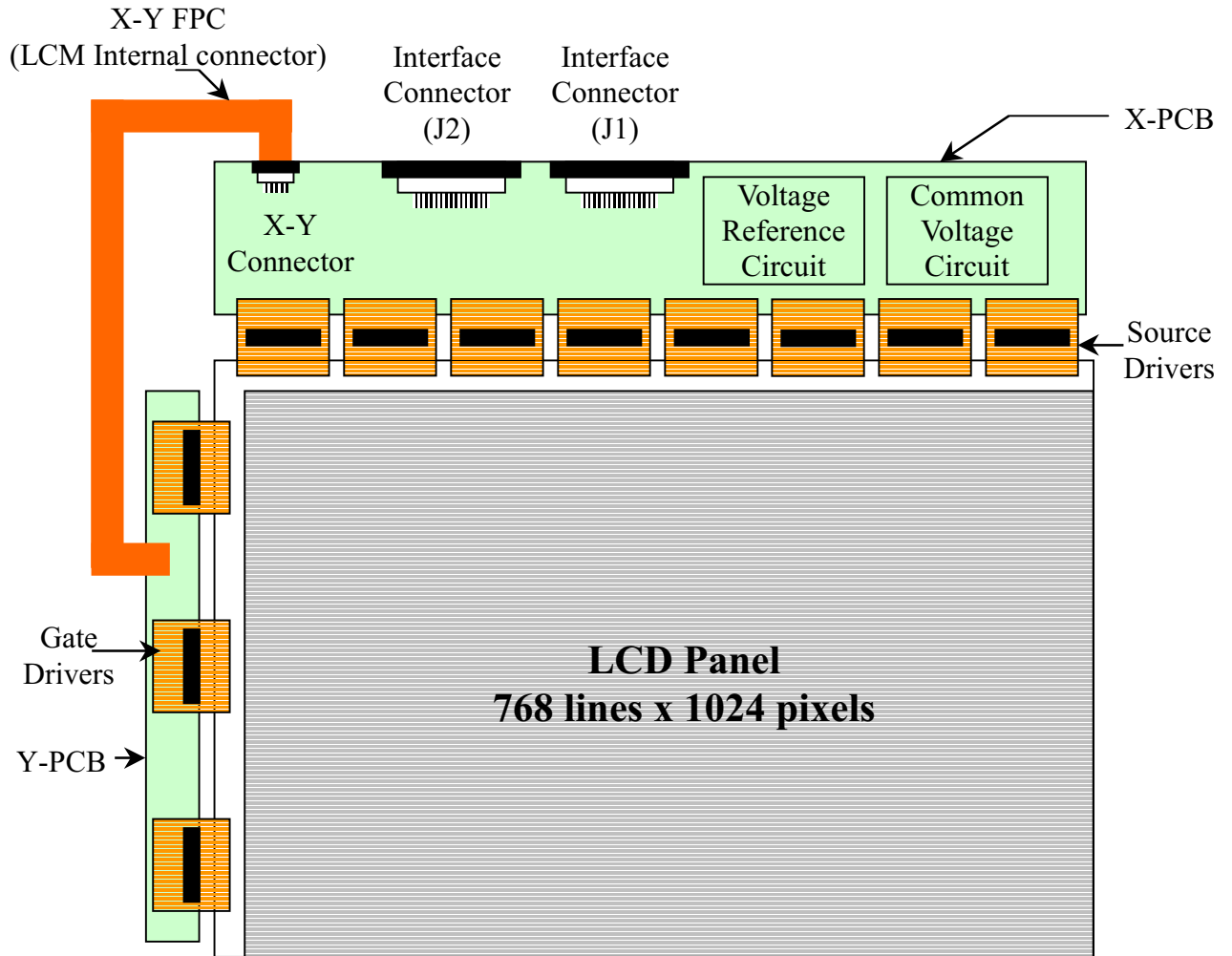
L63 : Luminance with all pixels white



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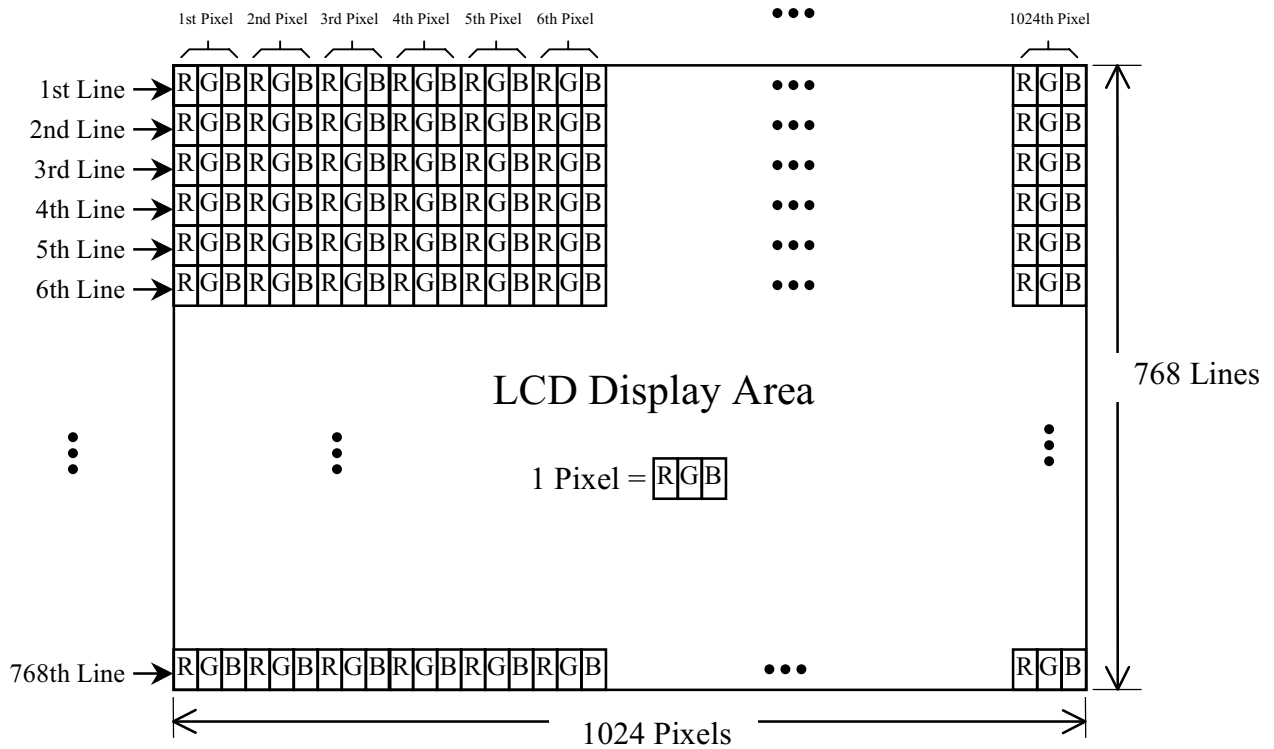
## 4.0 BLOCK DIAGRAM

### 4.1 LCD Module Block Diagram:



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### 4.2 Pixel Format



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### 4.3 Relationship between Displayed Color and Input Data

	Display	MSB						LSB						Gray scale level						
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0		B5	B4	B3	B2	B1	B0
Basic color	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	-
	Blue	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	-
	Green	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	-
	Light Blue	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	-
	Red	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	-
	Purple	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	H	H	-
	Yellow	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	-
	White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	-
Gray scale of Red	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark ↑ ↓ Light	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L1
		L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	L3...L60
		H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L61
	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L62	
	Red	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	Red L63
	Gray scale of Green	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Dark ↑ ↓ Light		L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L1
		L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	L3...L60
		L	L	L	L	L	L	H	H	H	H	L	H	L	L	L	L	L	L	L61
L		L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L62	
Green		L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	Green L63
Gray scale of Blue		Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	Dark ↑ ↓ Light	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L1
		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	L3...L60
		L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H	L61
	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	L62	
	Blue	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	Blue L63
	Gray scale of White and Black	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Dark ↑ ↓ Light		L	L	L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	H	L1
		L	L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	H	L	L2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	L3...L60
		H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	H	L61
H		H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	L62	
White		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	White L63

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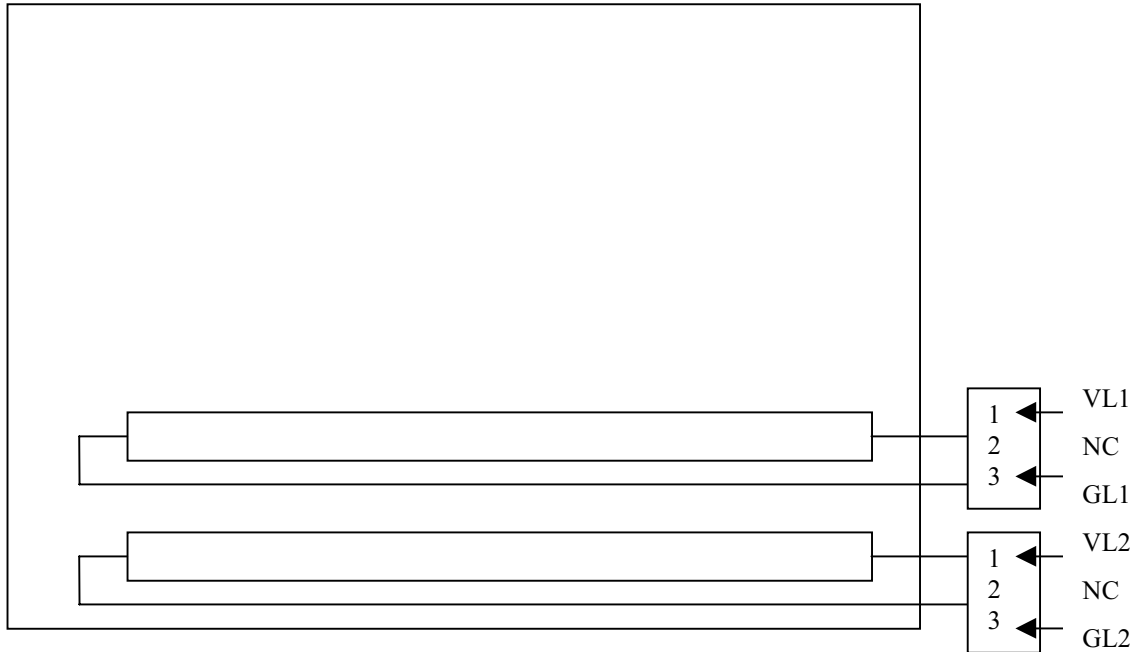
## 5.0 I/O CONNECTION PIN ASSIGNMENT

### 5.1 Interface FPC Connector (40-pins x 2) (Hirose: FH12-40S-0.5SH):

I/F FRC Connector (J1)			I/F FRC Connector (J2)		
Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	VDD2	Analog Power Input (DC +9V)	1	VDD1	Digital Power Input (DC +3.3V)
2	VDD2	Analog Power Input (DC +9V)	2	VDD1	Digital Power Input (DC +3.3V)
3	GND	Ground	3	GND	Ground
4	GND	Ground	4	GND	Ground
5	EB5	Even-dot Blue Data bit 5 (MSB)	5	OB5	Odd-dot Blue Data bit 5 (MSB)
6	EB4	Even-dot Blue Data bit 4	6	OB4	Odd-dot Blue Data bit 4
7	EB3	Even-dot Blue Data bit 3	7	OB3	Odd-dot Blue Data bit 3
8	EB2	Even-dot Blue Data bit 2	8	OB2	Odd-dot Blue Data bit 2
9	EB1	Even-dot Blue Data bit 1	9	OB1	Odd-dot Blue Data bit 1
10	EB0	Even-dot Blue Data bit 0 (LSB)	10	OB0	Odd-dot Blue Data bit 0 (LSB)
11	GND	Ground	11	GND	Ground
12	EG5	Even-dot Green Data bit 5 (MSB)	12	OG5	Odd-dot Green Data bit 5 (MSB)
13	EG4	Even-dot Green Data bit 4	13	OG4	Odd-dot Green Data bit 4
14	EG3	Even-dot Green Data bit 3	14	OG3	Odd-dot Green Data bit 3
15	EG2	Even-dot Green Data bit 2	15	OG2	Odd-dot Green Data bit 2
16	EG1	Even-dot Green Data bit 1	16	OG1	Odd-dot Green Data bit 1
17	EG0	Even-dot Green Data bit 0 (LSB)	17	OG0	Odd-dot Green Data bit 0 (LSB)
18	GND	Ground	18	GND	Ground
19	ER5	Even-dot Red Data bit 5 (MSB)	19	OR5	Odd-dot Red Data bit 5 (MSB)
20	ER4	Even-dot Red Data bit 4	20	OR4	Odd-dot Red Data bit 4
21	ER3	Even-dot Red Data bit 3	21	OR3	Odd-dot Red Data bit 3
22	ER2	Even-dot Red Data bit 2	22	OR2	Odd-dot Red Data bit 2
23	ER1	Even-dot Red Data bit 1	23	OR1	Odd-dot Red Data bit 1
24	ER0	Even-dot Red Data bit 0 (LSB)	24	OR0	Odd-dot Red Data bit 0 (LSB)
25	GND	Ground	25	GND	Ground
26	CPH1	Pixel Clock Input	26	CPH2	Pixel Clock Input
27	GND	Ground	27	GND	Ground
28	GND	Ground	28	GND	Ground
29	STH	Horizontal Start Pulse	29	NC	No Connecting
30	LOAD	Source Driver Latch Pulse	30	NC	No Connecting
31	POL	Source Driver Output Polarity control	31	VGH	Gate Driver High Voltage Input
32	REV	Data Reverse Control Signal	32	NC	No Connecting
33	GND	Ground	33	VGL	Gate Driver Low Voltage Input
34	GND	Ground	34	NC	No Connecting
35	STV1	Vertical Start Pulse 1	35	VGC	Gate Driver Common Voltage Input
36	STV2	Vertical Start Pulse 2	36	NC	No Connecting
37	CPV	Vertical Clock Input	37	NC	No Connecting
38	OE	Gate Driver Output Enable Signal	38	NC	No Connecting
39	GND	Ground	39	GND	Ground
40	GND	Ground	40	GND	Ground

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**5.2 Back Light Unit (CCFL) Connectors:**



BHR-03VS-1 / JAPAN SOLDERLESS TERMINAL MFG CO., LTD.

Mating Connector: SM02 (8.0) B-BHS/JAPAN SOLDERLESS TERMINAL MFG CO., LTD.

Terminal no.	Symbol	Function
1	VL1	CCFL power supply (high voltage)
2	NC	
3	GL1	CCFL power supply (low voltage)

BHR-03VS-1 / JAPAN SOLDERLESS TERMINAL MFG CO., LTD.

Mating Connector: SM02 (8.0) B-BHS/JAPAN SOLDERLESS TERMINAL MFG CO., LTD.

Terminal no.	Symbol	Function
1	VL2	CCFL power supply (high voltage)
2	NC	
3	GL2	CCFL power supply (low voltage)

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## 6.0 Electrical Characteristics:

### 6.1 Electrical system of TFT LCD Module:

Item	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Voltage	$V_{DD1}$	—	+3.0	+3.3	+3.6	V(DC)
	$V_{GH}$		<b>+23.0</b>	+23.5	<b>+24.0</b>	
	$V_{DD2}$		<b>+8.6</b>	+9.0	<b>+9.4</b>	
	$V_{GC}$		<b>-13.8</b>	-13.5	<b>-13.2</b>	
	$V_{GL}$		-6.3	-6.0	-5.7	
DC Load Input Current	<b><math>I_{in}(V_{DD1})</math></b>	—	—	<b>200</b>	<b>300</b>	mA
	<b><math>I_{in}(V_{GH})</math></b>		—	5.0	10.0	
	<b><math>I_{in}(V_{DD2})</math></b>		—	160.0	220.0	
	<b><math>I_{in}(V_{GC})</math></b>		—	10.0	20.0	
	<b><math>I_{in}(V_{GL})</math></b>		—	10.0	20.0	
DC Load Ripple Voltage	<b><math>V_{rpl}(V_{DD1})</math></b>	—	—	—	<b>50.0</b>	mVp-p
	$V_{rpl}(V_{GH})$		—	—	50.0	
	$V_{rpl}(V_{DD2})$		—	—	50.0	
	$V_{rpl}(V_{GC})$		—	—	50.0	
	$V_{rpl}(V_{GL})$		—	—	50.0	
Input Signal voltage	$V_{IH}$	High Level	<b>0.7 <math>V_{DD1}</math></b>	—	<b><math>V_{DD1}</math></b>	V
	$V_{IL}$	Low Level	0	—	<b>0.3 <math>V_{DD1}</math></b>	V

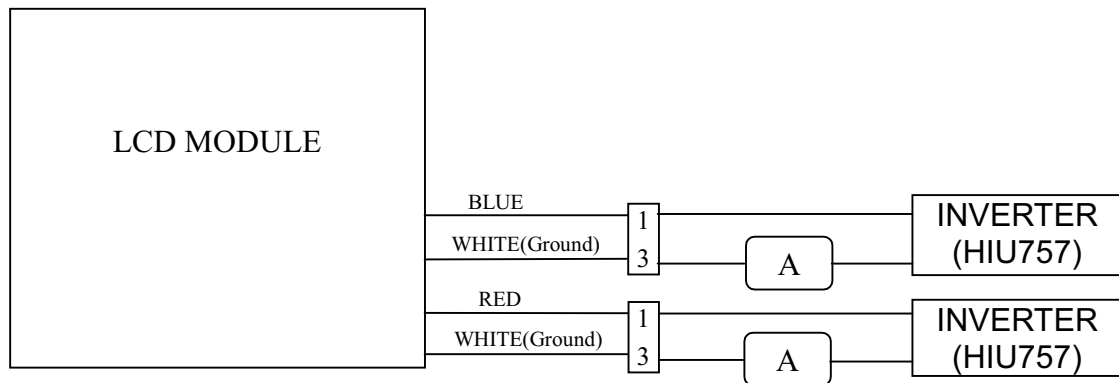
### 6.2 Back-Light Unit:

The back-light system is an edge-lighting type with 2-CCFL (Cold Cathode Fluorescent Lamp). The characteristics of two lamps are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Lamp current	$I_L$	3.0	6.0	7.0	mA(rms)	(1)
Lamp voltage	$V_L$	—	TBD	—	V(rms)	$I_L = \text{TBD mA}$
Frequency	$f_L$	20	50	70	KHz	(2)
Operating life time	Hr	30,000	—	—	Hour	(3)
Startup voltage	$V_s$	—	—	1220	V(rms)	at 25°C
				1410		at 0°C

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Note: (1) Lamp current is measured with current meter for high frequency as shown below. Specified values are for a lamp.



- (2) Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency shall be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.
- (3) Life time (Hr) can be defined as the time in which it continues to operate under the condition:  $T_a=25\pm 3^\circ\text{C}$ ,  $I_L=6.0\text{mA(rms)}$  and  $f_L=50\text{ KHz}$  until one of the following event occurs:
1. When the brightness becomes 50%.
  2. When the startup voltage ( $V_s$ ) at  $0^\circ\text{C}$  becomes higher than the maximal value of  $V_s$  specified above.

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### 6.3 AC Electrical Characteristics:

#### 6.3.1 AC Timing: (VDD1=3.0V~3.6V, TOPR=25 oC) 5)

Item	Symbol	Min.	Typ.	Max.	Unit	Signals	Note
Reference Signal (Pixel Clock)	F1	50	65	80	MHz		
	T1=CLK	12.5	15.384	20	n-Sec		
	T2=T1*2	25	30.769	40	n-Sec		
Reference Signal (DENB)	Line Periodic	T3=Line	<b>526</b>	672	<b>900</b>	T2	1), 2), 4)
	Line Active	T4	512	512	512	T2	
	Line Blank	T5	<b>14</b>	160	<b>388</b>	T2	
	Frame Periodic	T6	<b>773</b>	806	<b>950</b>	Lines	
	Frame Active	T7	768	768	768	Lines	
	Frame Blank	T8	<b>5</b>	---	---	Lines	
Vertical Periodic	Periodic	T6	<b>773</b>	806	<b>950</b>	Lines	STV1 STV2 2)
	Pulse Width	T9	1	1	---	Lines	
		T10	2	2	---	---	
	Rising Time	T11	---	40	60	n-Sec	
	Falling Time	T12	---	40	60	n-Sec	
	Set-up Time	T13	700	800	---	n-Sec	
Horizontal Periodic	Hold Time	T14	700	800	---	n-Sec	OE CPV LOAD STH  LOAD STH
	Period	T15	---	1	---	Lines	
	Pulse Width	T16A	1			u-Sec	
		T16B	1			u-Sec	
		T16C	2	64	100	T2	
		T16D	25	30.769	40	n-Sec	
	Rising Time	T17A		40	60	n-Sec	
		T17B		40	60		
		T17C	2	4			
	Falling Time	T17D	2	4		n-Sec	
		T18A		40	60		
T18B			40	60			
T18C		2	4				
Set-up Time	T18D	2	4		n-Sec		
	T19A	7	10	---			
	T19B	7	10	---			
Hold Time	T20A	7	10	---	n-Sec		
	T20B	7	10	---			

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Item	Symbol	Min.	Typ.	Max.	Unit	Signals	Note
Horizontal Periodic	Period	T21	---	2	---	Lines	POL
	Pulse Width	T22	---	1	---	Lines	
	Rising Time	T23	7	10	---	n-Sec	
	Falling Time	T24	7	10	---	n-Sec	
	Set-up Time	T25	-5	---	---	n-Sec	
	Hold Time	T26	6	---	---	n-Sec	
Clock	Period	T2	25.00	30.769	40	n-Sec	CPH1 CPH2
	Rising Time	T27	2	4	---	n-Sec	
	Falling Time	T28	2	4	---	n-Sec	
Image Data And Data Reverse Control Pin	Setup time	T29	2	---	---	n-Sec	ER(5:0) EG(5:0) EB(5:0) OR(5:0) OG(5:0) OB(5:0) REV
	Hold time	T30	2	---	---	n-Sec	
Relative Signals	LOAD rising-STH rising	T31	2	---	---	n-Sec	
	CPV rising-LOAD rising	T32	2	4	---	u-Sec	

Note 1) Refer to VESA standard.

Note 2) In case of using the long frame period, the deterioration of display quality, noise etc. may be occurred.

Note 3) Do not fix CPH1 and CPH2 to “H” or “L” level while the  $V_{DD}$  (+3.3V) is supplied. If CPH1 and CPH2 is fixed to “H” level or “L” level for certain period while the  $V_{DD}$  (+3.3V) is supplied, the panel may be damaged.

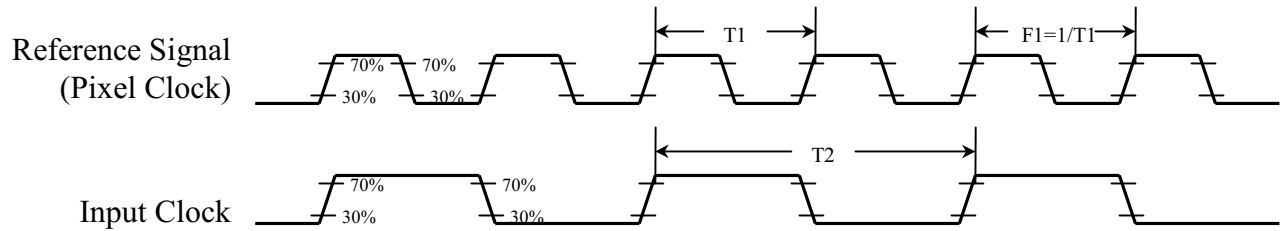
Note 4) Do not change t3 and t6 values in the operation. When t1 or t4 is changed, the panel is displayed as black.

Note 5) Please adjust LCD operating signal timing and FL driving frequency, to optimize the display quality. There is a possibility that flicker is observed by the interference of LCD operating signal timing and FL driving condition (especially driving frequency).

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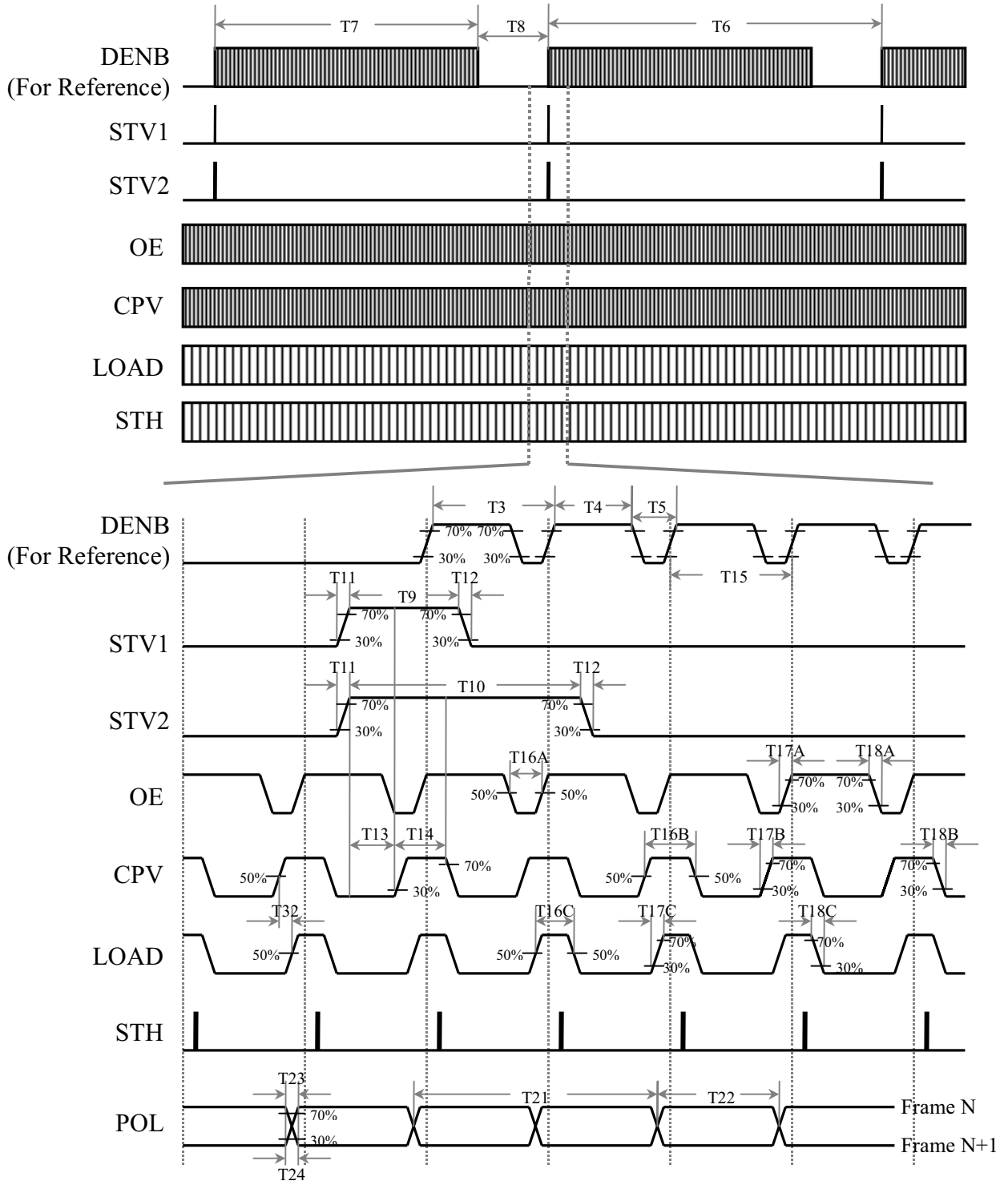
### 6.3.2 AC Timing Charts:

(1). Reference Signal (pixel clock):



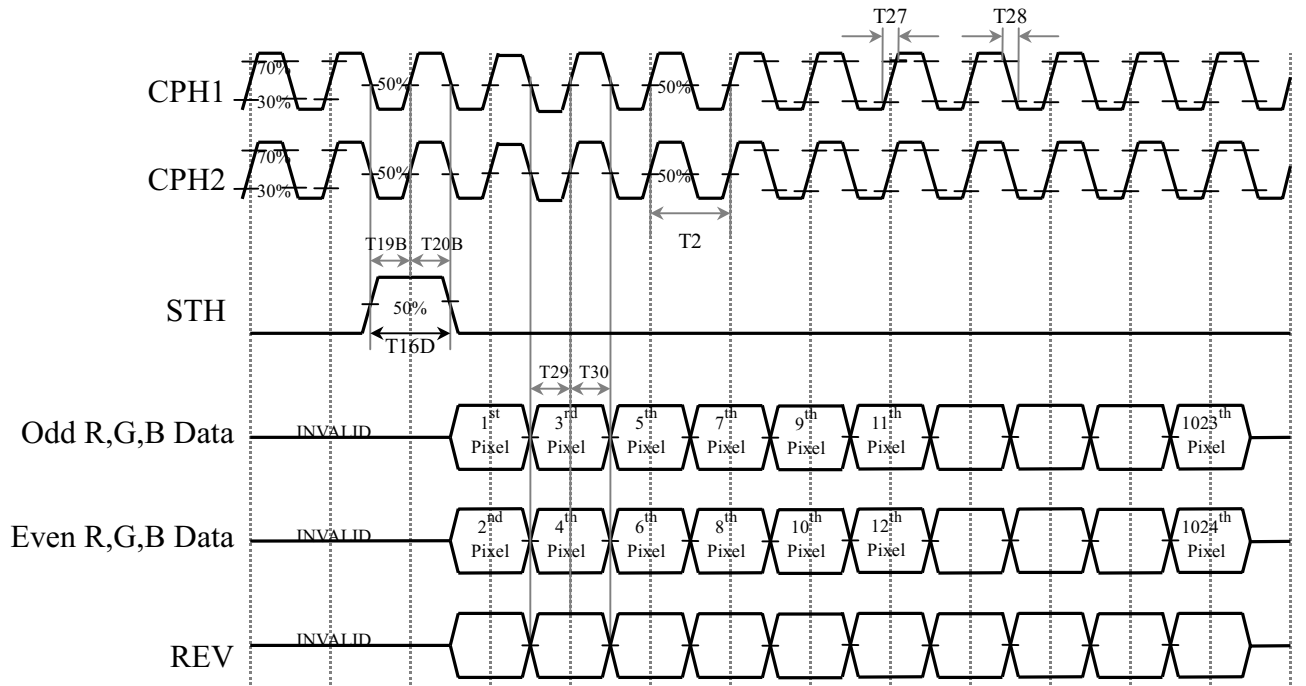
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(2). Vertical Periodic (STV1, STV2, OE, CPV):

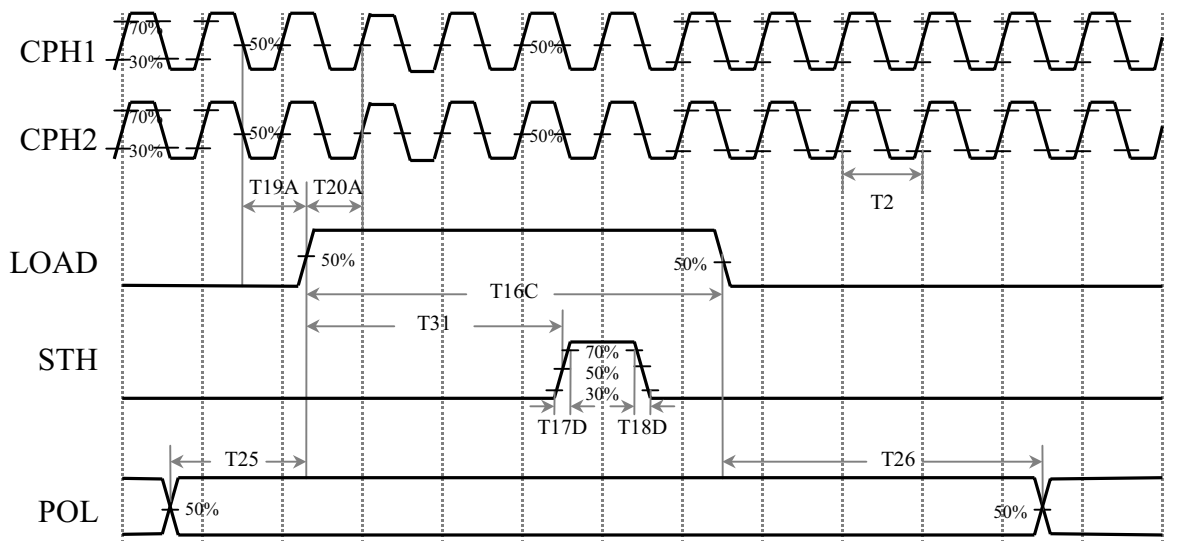


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(3). Horizontal Periodic 1 (STH, CPH, DATA):



(4). Horizontal Periodic 2 (CPH, LOAD, STH, POL):



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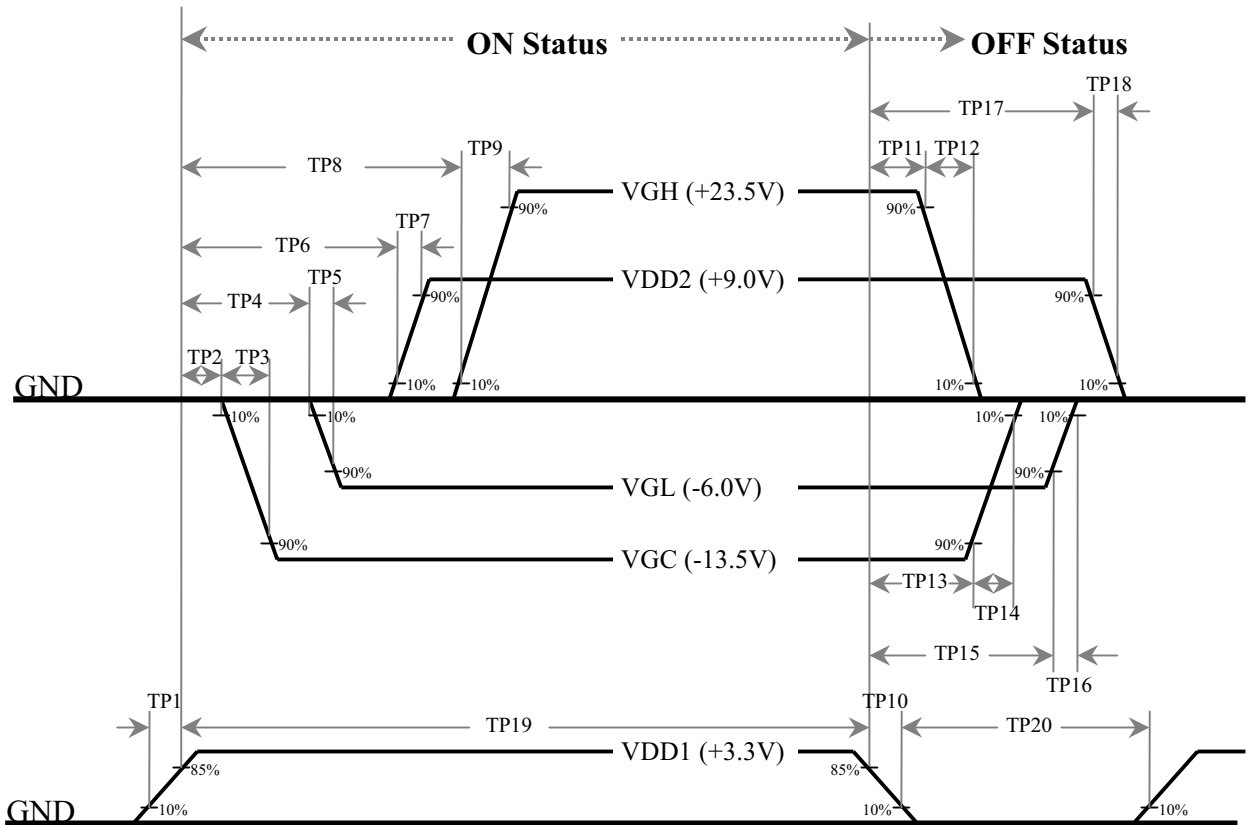
**6.4 Power Sequence :**

**6.4.1 Power Sequence Timing Specification**

Statu s	Item	Symbol	Min.	Typ.	Max.	Unit	Note
ON	VDD1 (3.3V) Input Power Rising Time	TP1	0.3	0.5	---	m-sec	
	VGC (-13.5V) ON Delay Time	TP2	5	7	---	m-sec	
	VGC (-13.5V) Input Power Falling Time	TP3	1	2	---	m-sec	
	VGL (-6.0V) ON Delay Time	TP4	5	7	---	m-sec	
	VGL (-6.0V) Input Power Falling Time	TP5	0.8	1	---	m-sec	
	VDD2 (+9.0V) ON Delay Time	TP6	6	8	---	m-sec	
	VDD2 (+9.0V) Input Power Rising Time	TP7	1.5	2	---	m-sec	
	VGH (+23.5V) ON Delay Time	TP8	5	8	---	m-sec	
	VGH (+23.5V) Input Power Rising Time	TP9	3	4	---	m-sec	
OFF	VDD1 (3.3V) Input Power Falling Time	TP10	100	300	---	m-sec	
	VGH (+23.5V) OFF Delay Time	TP11	---	0.5	1	m-sec	
	VGH (+23.5V) Input Power Falling Time	TP12	100	300	---	m-sec	
	VGC (-13.5V) OFF Delay Time	TP13	---	0.5	1	m-sec	
	VGC (-13.5V) Input Power Rising Time	TP14	100	300	---	m-sec	
	VGL (-6.0V) OFF Delay Time	TP15	---	0.5	1	m-sec	
	VGL (-6.0V) Input Power Rising Time	TP16	100	300	---	m-sec	
	VDD2 (+9.0V) OFF Delay Time	TP17	---	0.5	1	m-sec	
	VDD2 (+9.0V) Input Power Falling Time	TP18	100	300	---	m-sec	
	ON Duty	TP19	500	---	---	m-sec	
	OFF Duty	TP20	500	---	---	m-sec	

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### 6.4.2 Input Voltage Power Sequence

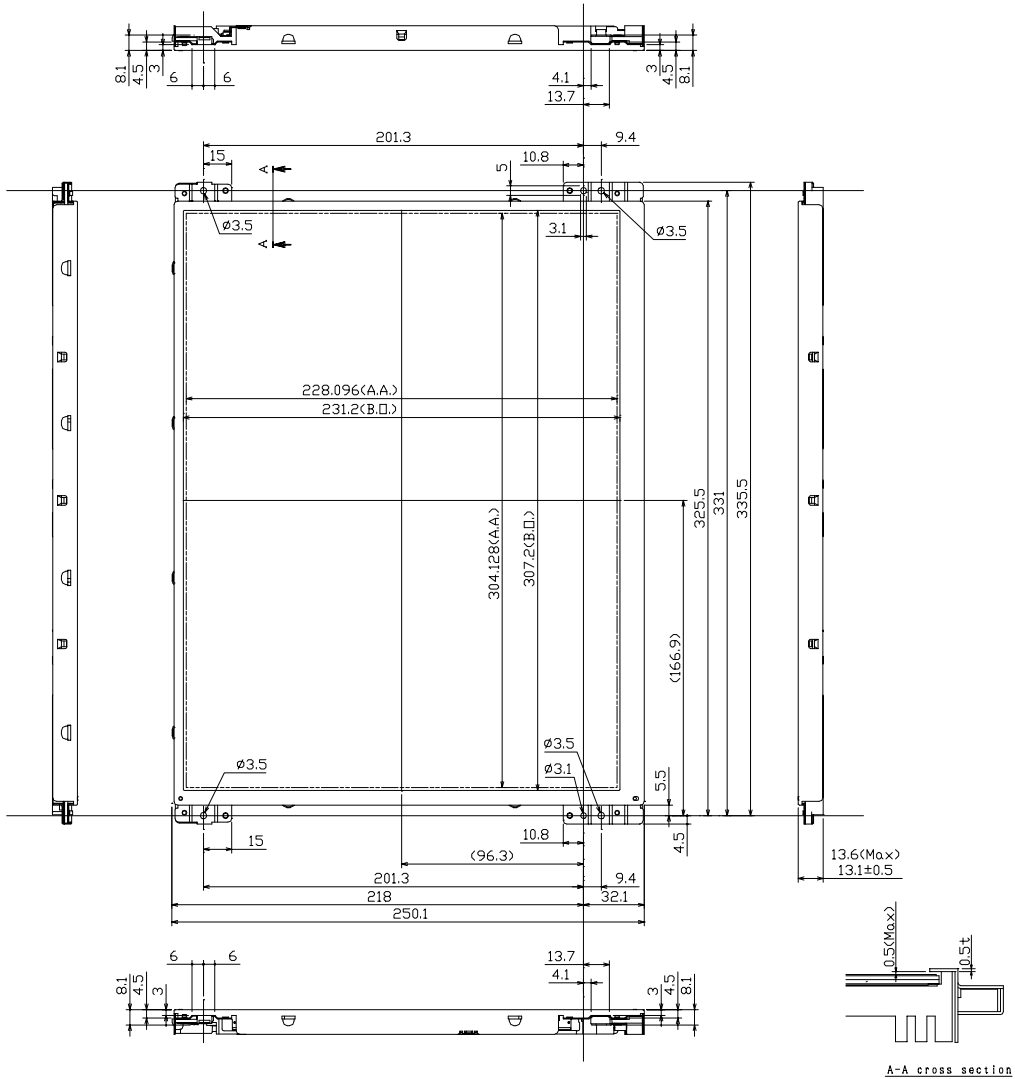


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## 7.0 OUTLINE DIMENSION

### 7.1 Front View:

Date: 20010518

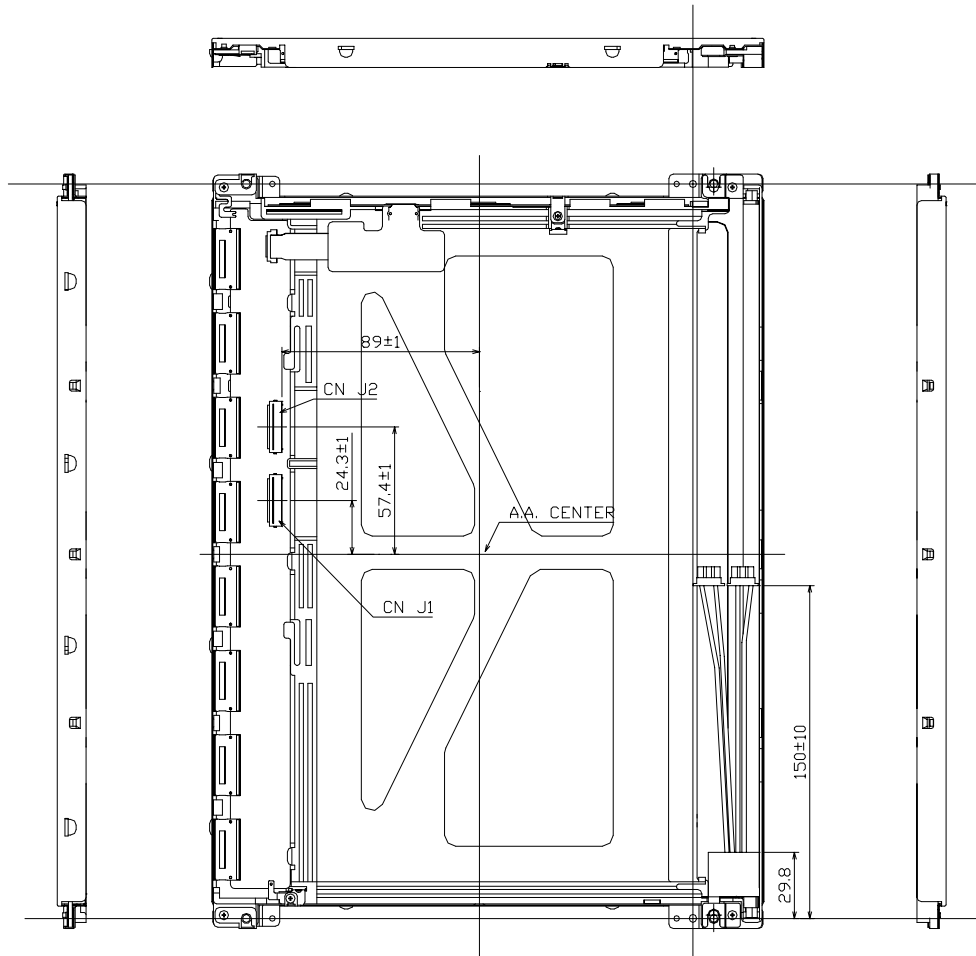


NOTE:  
1. UNSPECIFIED DIMENSIONAL TOLERANCE ARE ±0.5mm

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**7.2 Back View:**

**Date: 20010518**



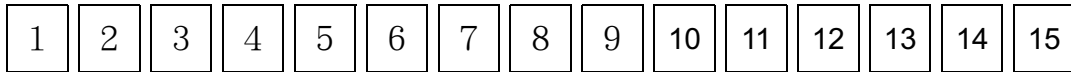
Note:

1. THE MAX HEIGHT VAULE IS MEASURED FROM STEEL BEZEL FRONT SURFACE.
2. UNSPECIFIED DIMENSIONAL TOLERANCE ARE  $\pm 0.5\text{mm}$
3. CONNECTOR: J1, J2 Type FH12-40S-0.5SH(HIROSE)

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## 8.0 LOT MARK

### 8.1 Lot Mark



code 1,2,3,4,5,6: HannStar internal flow control code.

code 7: production location.

code 8: production year.

code 9: production month.

code 10,11,12,13,14,15: serial number.

#### Note (1) Production Year

Year	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008
Mark	9	0	1	2	3	4	5	6	7	8

#### Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct.	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

### 8.2 Location of Lot Mark

- (1) The label is attached to the backside of the LCD module.
- (2) This is subject to change without prior notice.



Lot mark

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## 9.0 GENERAL PRECAUTION

### 9.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

### 9.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

### 9.3 Breakage of LCD Panel

- 9.3.1 If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.
- 9.3.2 If liquid crystal contacts mouth or eyes, rinse out with water immediately.
- 9.3.3 If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
- 9.3.4 Handle carefully with chips of glass that may cause injury, when the glass is broken.

### 9.4 Electric Shock

- 9.4.1 Disconnect power supply before handling LCD module.
- 9.4.2 Do not pull or fold the CCFL cable.
- 9.4.3 Do not touch the parts inside LCD modules and the fluorescent lamp's connector or cables in order to prevent electric shock.

### 9.5 Absolute Maximum Ratings and Power Protection Circuit

- 9.5.1 Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.
- 9.5.2 Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
- 9.5.3 It's recommended employing protection circuit for power supply.

### 9.6 Operation

- 9.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.
- 9.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
- 9.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.
- 9.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.
- 9.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.



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**9.7 Mechanism**

Please mount LCD module by using mounting holes arranged in four corners tightly.

**9.8 Static Electricity**

- 9.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.
- 9.8.2 Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge.
- 9.8.3 Persons who handle the module should be grounded through adequate methods.

**9.9 Strong Light Exposure**

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

**9.10 Disposal**

When disposing LCD module, obey the local environmental regulations.