

HITACHI

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FOR MESSRS: _____

DATE : Oct.31,2007

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

SP09Q02L0CLZZ

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* When product will be discontinued, customer will be informed by HITACHI with twelve months prior to discontinuation.

* This product is inhibited to apply in any life support instrument.

ACCEPTED BY: _____

PROPOSED BY: Dan Cheng

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RECORD OF REVISION

DATE	SHEET No.	SUMMARY

KAOSIUNG HITACHI
ELECTRONICS CO.,LTD.

DATE Oct.31,'07

Sh.
No.

7B64PS 2702- SP09Q02L0CLZZ-1

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3. GENERAL SPECIFICATIONS

(1) Part Name	SP09Q02L0CLZZ
(2) Module Size	89.0 (W)mm x 66.5 (H)mm x 5.5 (D)mm
(3) Active Area	71.985(W)mm x 47.985(H)mm
(4) Dot Size	0.30 (W)mm x 0.30 (H)mm
(5) Dot Pitch	0.285 (W)mm x 0.285 (H)mm
(6) Resolution	240 (W) x 160 (H) dots
(7) Duty Ratio	1/160
(8) Bias Ratio	1/9
(9) LCD Type	Transmissive type B/W F-STN (Negative Mode) with anti-glare type upper polarizer
(10) Viewing Direction	12 O'clock
(11) Backlight	White LED Life time : 35khr @25°C Note : Life time for half of initial brightness.

4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS.

VSS=0V:STANDARD

ITEM	SYMBOL	MIN.	MAX.	UNIT	COMMENT
Power Supply for Logic	VDD-VSS	-0.3	7.0	V	
Power Supply for LC Drive	VLCD	0	30.0	V	
Input Voltage	Vi	-0.3	VDD+0.3	V	(Note 1,2)

Note 1 : $\overline{\text{DOFF}}$, FLM , CL1 , CL2 , D0~D3 , M.

Note 2 : Make certain you are grounded when handling LCM.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS.

I T E M	OPERATING		STORAGE		COMMENT
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	0°C	70°C	-20°C	80°C	(Note 2,3,6)
Humidity	(Note 1)		(Note 1)		Without condensation
Vibration	-	2.45m/s ² (0.25G)	-	11.76m/s ² (1.2G) (Note 5)	1h max. (Note 4)
Shock	-	29.4m/s ² (3 G)	-	490.0m/s ² (50 G) (Note 5)	X · Y · Z Directions
Corrosive Gas	Not acceptable		Not acceptable		

Note 1 : Ta ≤ 40°C : 85%RH max.

Ta > 40°C : Absolute humidity must be lower than the humidity of 85%RH at 40°C

Note 2 : Ta at -20°C < 48h , at 80°C < 168h.

Note 3 : Background color changes slightly depending on ambient temperature.
This phenomenon is reversible.

Note 4 : 5Hz~100Hz (Except resonance frequency)

Note 5 : This module should be operated normally after finish the test.

Note 6 : The operating temperature only guarantee the display can be operated ; regarding the contrast , response time , brightness and other features related to the quality are judged by Ta=25°C condition .

5. ELECTRICAL CHARACTERISTICS

5.1 ELECTRICAL CHARACTERISTICS OF LCD

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage for Logic	VDD-VSS	-	2.5	3.3	4.5	V
Power Supply Voltage for LCD Driving	VLCD-VSS	-	-	-	30.0	V
Input Voltage (Note 1)	Vi	H level	0.8VDD	-	VDD	V
		L level	0	-	0.2VDD	V
Power Supply Current For Logic , (Note 2)	IDD	VDD-VSS=3.3V VLCD-VSS=(16.2)V	-	0.02	-	mA
Power Supply Current for LC Driving , (Note 2)	ILCD	VDD-VSS=3.3V VLCD-VSS=(16.2)V	-	0.1	-	mA
Recommended LC Driving Voltage (Note 3)	VLCD-VSS	Ta= 0°C , $\phi=0^\circ$	-	17.2	-	V
		Ta=25°C , $\phi=0^\circ$	-	16.2	-	V
		Ta=50°C , $\phi=0^\circ$	-	15.2	-	V
Frame Frequency (Note 4)	fFLM	-	70	75	80	Hz

Note 1 : \overline{DOFF} , FLM , CL1 , CL2, D0~D3,M.

Note 2 : fFLM=75Hz , Test pattern is all "Q".

VLCD-VSS=16.2V, Ta=25°C.

Note 3 : Recommended LC driving voltage change about $\pm 1.0V$ by each module.
Test pattern is all "Q".

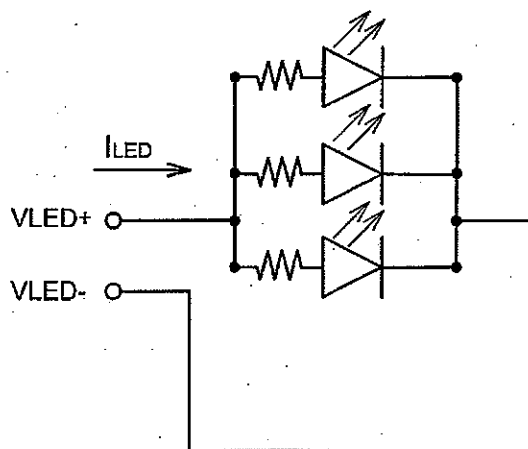
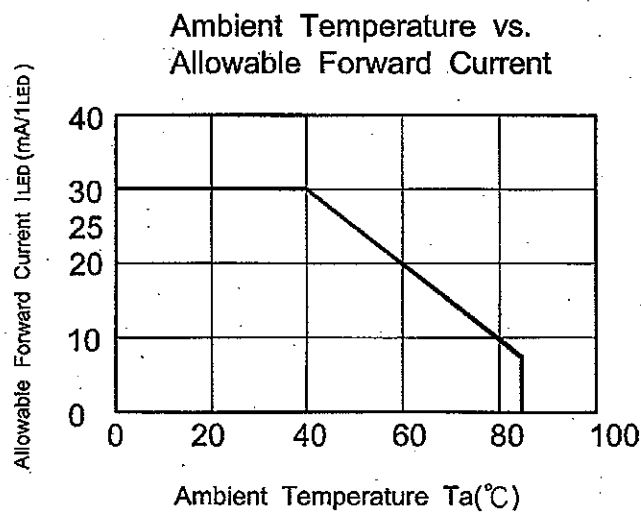
Note 4 : Need to make sure of flicking and rippling of display when setting the frame frequency in your set.

5.5 ELECTRICAL CHARACTERISTICS OF LED BACKLIGHT

Ta=25°C (Backlight on)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage for LED	VLED	-	-	5.0	5.2	V
Power Supply Current for LED	ILED	VLED=5.0V	-	(60)	75 (Note 1)	mA

Note 1 : The ILED changes depending on ambient temperature.



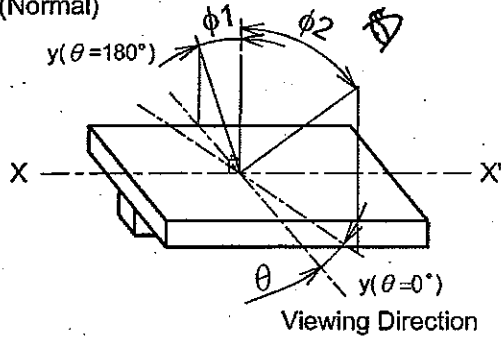
6. OPTICAL CHARACTERISTICS

6.1 OPTICAL CHARACTERISTICS OF LCD

Ta=25°C (Backlight on)

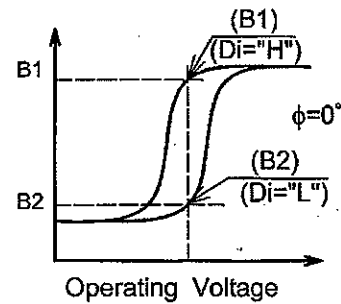
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Viewing Angle	$\phi_2-\phi_1$	$K \geq 2.0$	-	80	-	deg.	1,2
Contrast Ratio	K	$\phi=0^\circ, \theta=0^\circ$	-	30	-	-	3
Response Time (Rise)	tr	$\phi=0^\circ, \theta=0^\circ$	-	150	-	ms	4
Response Time (Fall)	tf	$\phi=0^\circ, \theta=0^\circ$	-	350	-	ms	4

Note 1 : Definition of θ and ϕ
(Normal)

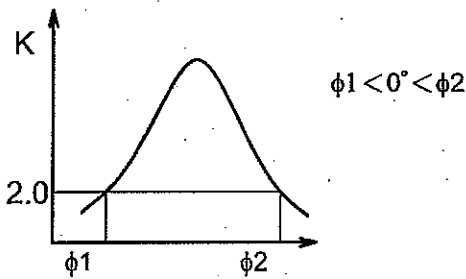


(Measure condition by HITACHI)
Note 3 : Definition of contrast "K"

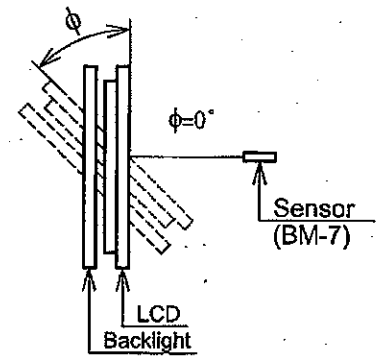
$$K = \frac{\text{Brightness on selected dot (B1)}}{\text{Brightness on non-selected dot (B2)}}$$



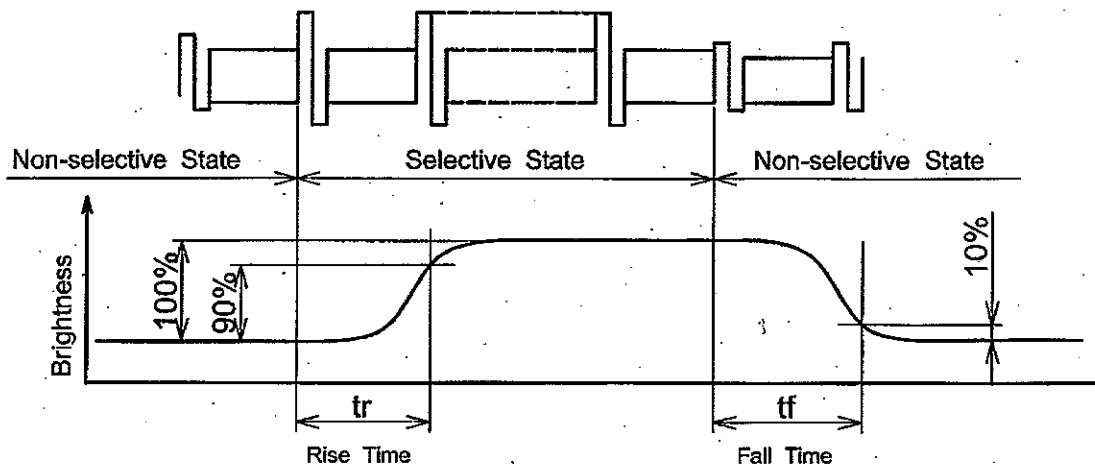
Note 2 : Definition of viewing angle ϕ_1 and ϕ_2



Contrast ratio K vs viewing angle ϕ



Note 4 : Definition of optical response

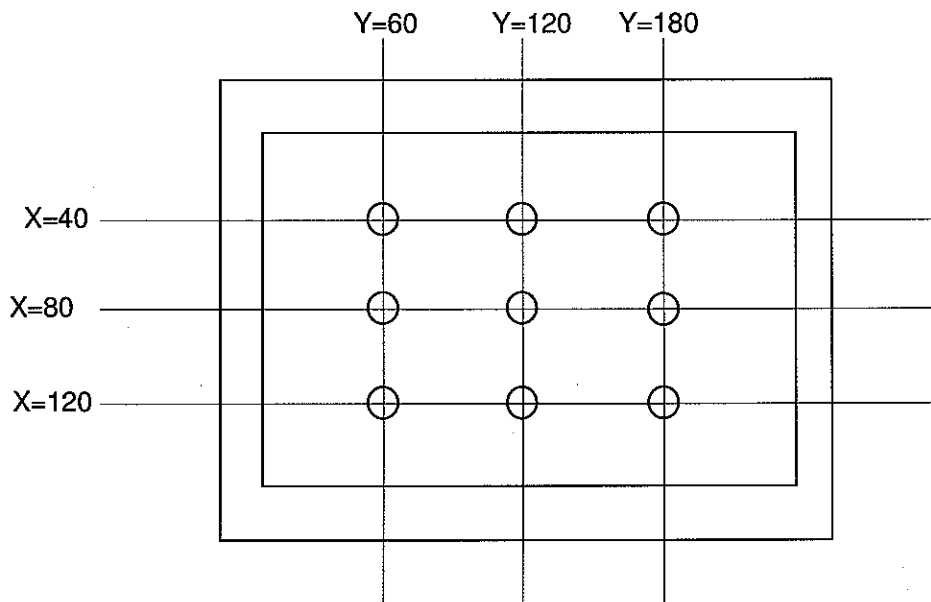


6.2 OPTICAL CHARACTERISTICS OF BACKLIGHT

(LCM, BACKLIGHT ON, Ta=25°C)

ITEM	MIN.	TYP.	MAX.	UNIT	NOTE
Brightness Uniformity	-	-	±35	%	(Note 1,2)
Brightness	-	90	-	cd/m ²	I _{LED} =60 mA

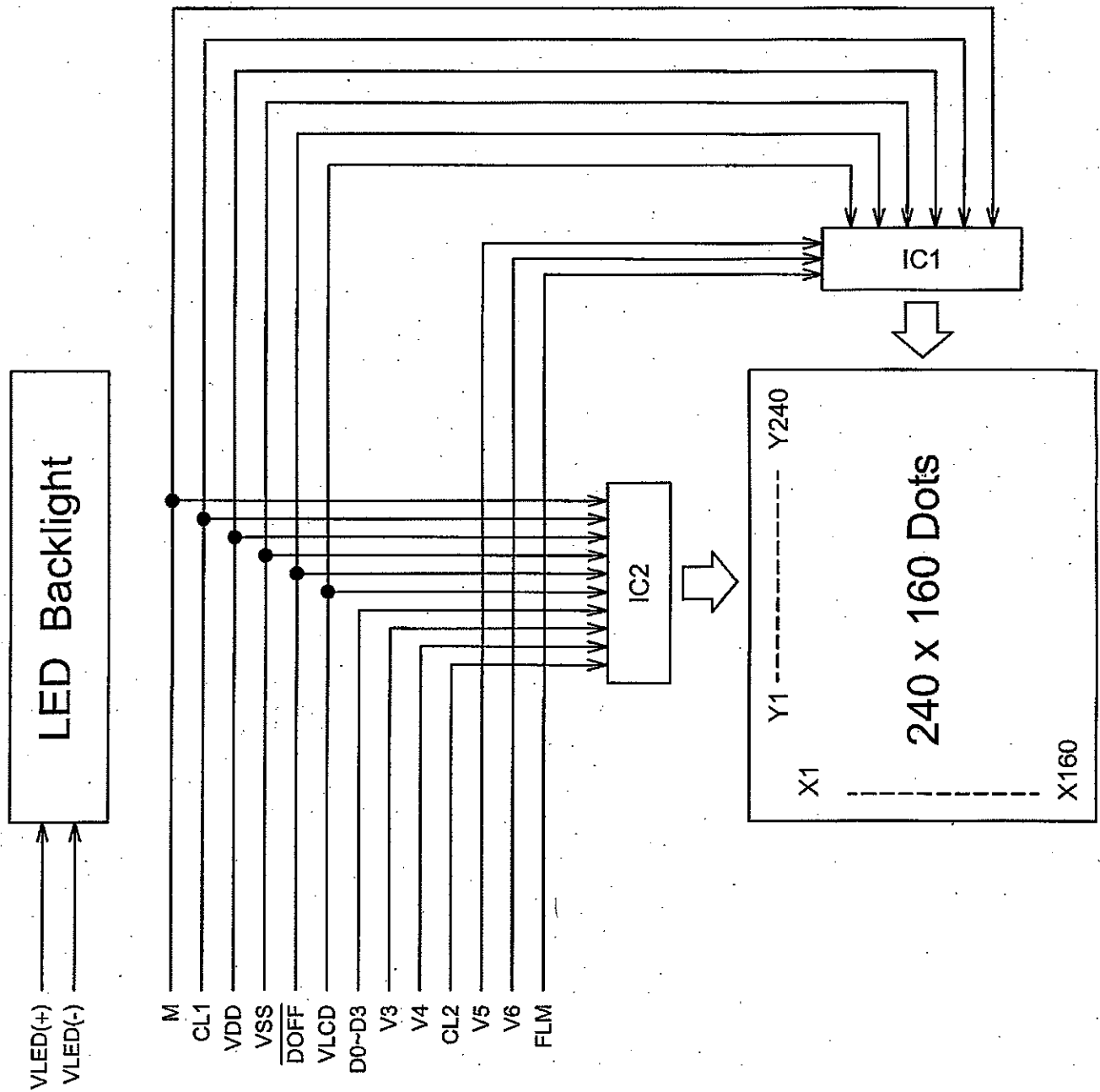
Note 1 : Measure of the following 9 places on the display.



Note 2 : Definition of brightness tolerance.

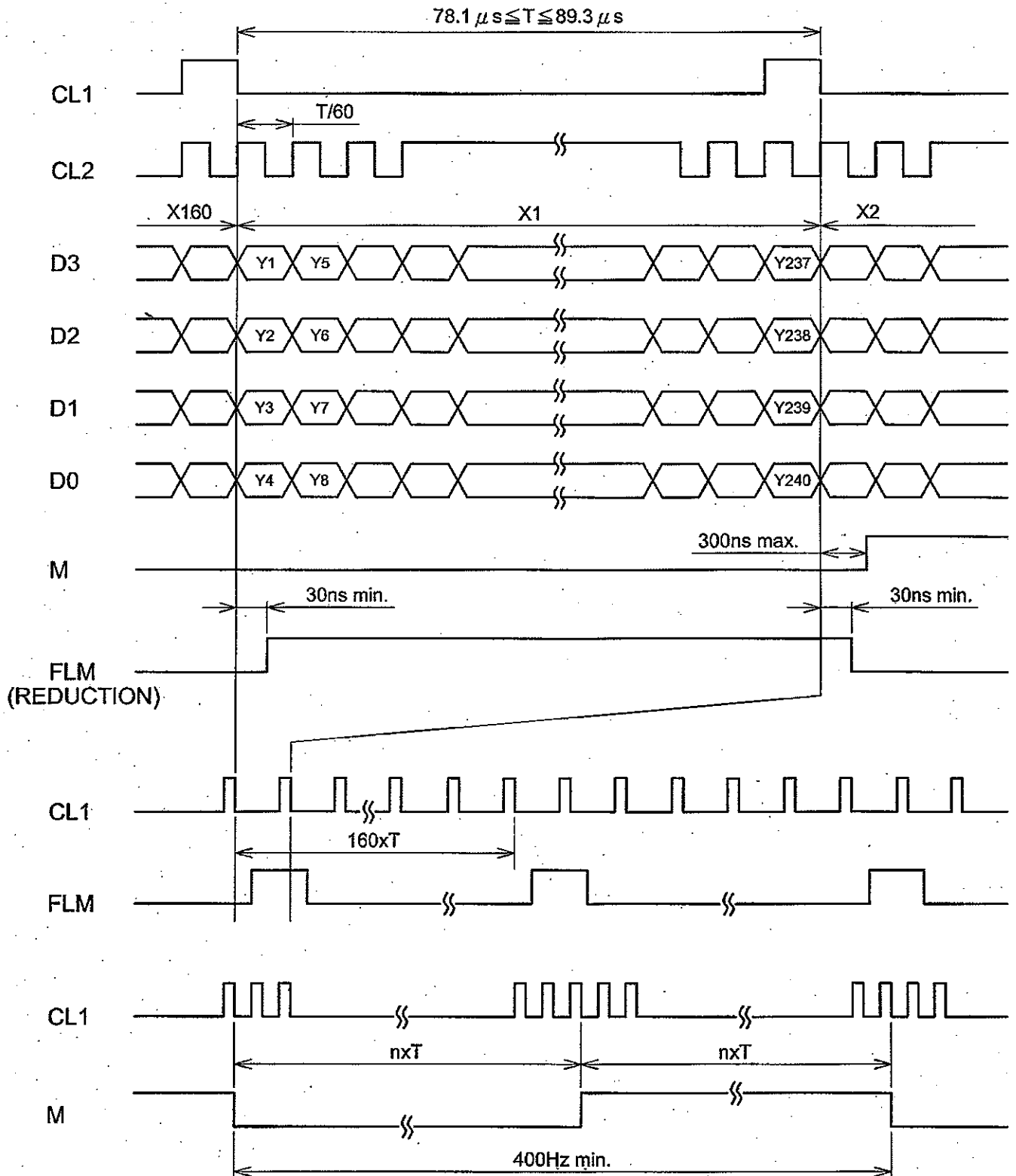
$$\left(\frac{\text{Max. or Min. Brightness} - \text{Average Brightness}}{\text{Average Brightness}} \right) \times 100\%$$

7. BLOCK DIAGRAM



8. INTERFACE TIMING

8.1 TIMING CHART (4-BITS PARALLEL DATA INPUT)



Note 1 : M signal should be kept 400Hz min. and 50% duty.

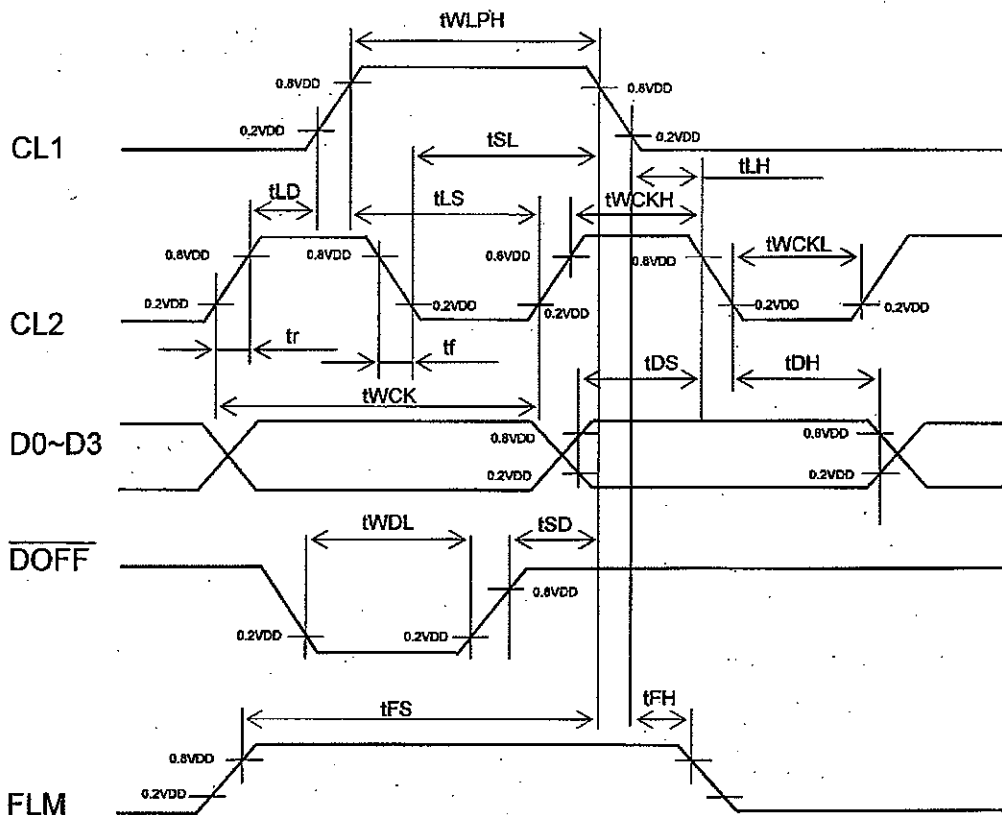
Note 2 : HITACHI recommend $nxCL1$ pulses of M signal 50%.

$n=13$

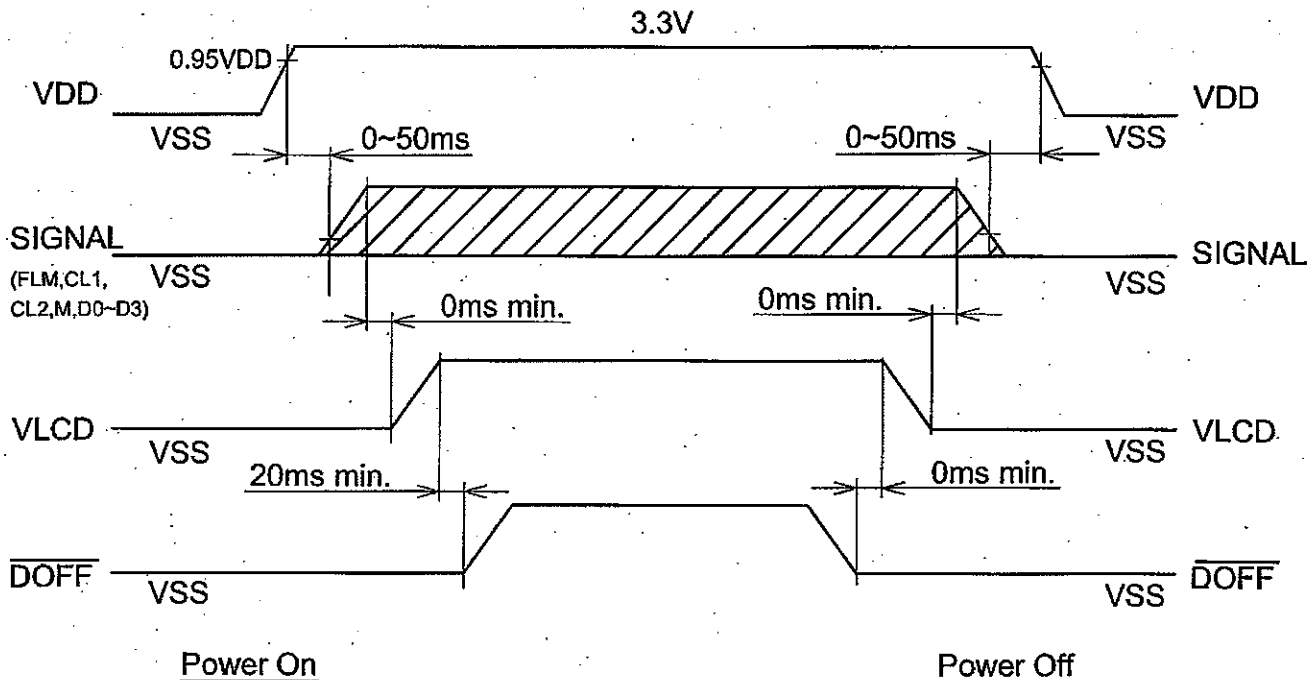
8.2 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Shift Clock Period	tWCK	125	-	-	ns	$t_r, t_f \leq 11\text{ns}$
Shift Clock "H" Pulss Width	tWCKH	51	-	-	ns	
Shift Clock "L" Pulss Width	tWCKL	51	-	-	ns	
Data Setup Time	tDS	30	-	-	ns	
Data Hole Time	tDH	40	-	-	ns	
Latch Pulse "H" Pulse Width.	tWLPH	51	-	-	ns	
Shift Clock Rise to Latch Pulse Rise Time	tLD	0	-	-	ns	
Shift Clock Rise to Latch Pulse Fall Time	tSL	51	-	-	ns	
Latch Pulse Rise to Shift Clock Rise Time	tLS	51	-	-	ns	
Latch Pulse Fall to Shift Clock Fall Time	tLH	51	-	-	ns	
Input Signal Rise Time	t_r	-	-	50	ns	(Note 1)
Input Signal Fall Time	t_f	-	-	50	ns	(Note 1)
DOFF Removal Time	tSD	100	-	-	ns	
DOFF Enable Pulse Time	tWDL	1.2	-	-	μs	
"FLM" Set Up Time	tFS	100	-	-	ns	
"FLM" Hold Time	tFH	30	-	-	ns	

Note 1 : $(t_{WCK} - t_{WCKH} - t_{WCKL}) / 2$ is the maximum in the case of high speed operation.



8.3 TIMING OF POWER SUPPLY AND INTERFACE SIGNAL



Note 1: $\overline{\text{DOFF}}$ function takes priority even if the input signal status becomes irregular immediately after VDD power-on.

Note 2: Please keep the specified sequence because wrong sequence may cause permanent damage to the LCM.

8.4 POWER SUPPLY FOR LCM

