

Engineering Specification

**Type 18.1 SXGA Monochrome TFT/LCD Module
Model Name:ITSX88E4**

Document Control Number : OEM I-88E4-01

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

**Sales Support
International Display Technology**

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ii Record of Revision

| Date | Document Revision | Page | Summary |
|-------------|-------------------|------|-----------------------------|
| July 4,2002 | OEM I-88E4-01 | All | First Edition for customer. |

1.0 Handling Precautions

- Damage to the panel or the panel electronics may result from any deviation from the recommended power on/off sequencing. The panel should not be hot plugged. Refer to the Power On/Off Sequence section in this Specification.
- Handle the panel with care. The LCD panel and CCFL (Cold Cathode Fluorescent Lamp)s are made of glass and may crack or break if dropped or subjected to excessive force.
- The CCFLs contain a small amount of Mercury so should not be disposed of to landfill. Dispose of as required by local ordinances or regulations.
- The LCD module contains small amounts of material having no flammability grade. The exemption conditions of the flammability requirements (4.7.3.4, IEC60950 3rd.Ed. or UL60950 3rd.Ed.) should be applied.
- The panel may be damaged by the application of twisting or bending forces to the module assembly. Care should be taken in the design of the monitor housing and the assembly procedure to prevent stress damage to the panel especially the lamp cable and the lamp connector..
- Use standard earthing/grounding procedures to prevent damage to the CMOS LSI while handling the module.
- Use earthing/grounding procedures, an ionic shower, or similar to prevent static damage while removing the protective front sheet.
- The front polarizer can be easily damaged. Take care not to scratch the front surface with any hard or abrasive material. Dust, finger marks, grease etc. can be removed with a soft damp cloth (a small amount of mild detergent can be used on the damp cloth). Do not apply water or detergent directly to the front surface as this may cause staining or damage the electronic components.
- Never use any solvent on the front polarizer or module as this may cause permanent damage.
- Do not open or modify the module assembly.
- Continuous operation of the panel with the same screen content may result in some image sticking. Over 10 hours operation with the same content is not recommended.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- Please do not use middle 3(three) screw holes on the upper(long) side and middle 3(three) screw holes on the lower(long) side for panel fixing. These screw holes are for manufacturing purpose only.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the Type 18.1 Monochrome TFT/LCD Module 'ITSX88E4'.

This module is designed for a LCD monitor style display unit. This module includes inverter card.

The screen format and electrical interface are intended to support the VESA SXGA (1280(H) x 1024(V) at 60Hz) screen.

Supported gray scale is 8-bit per 1(one) sub-pixel.

All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.

2.1 Characteristics

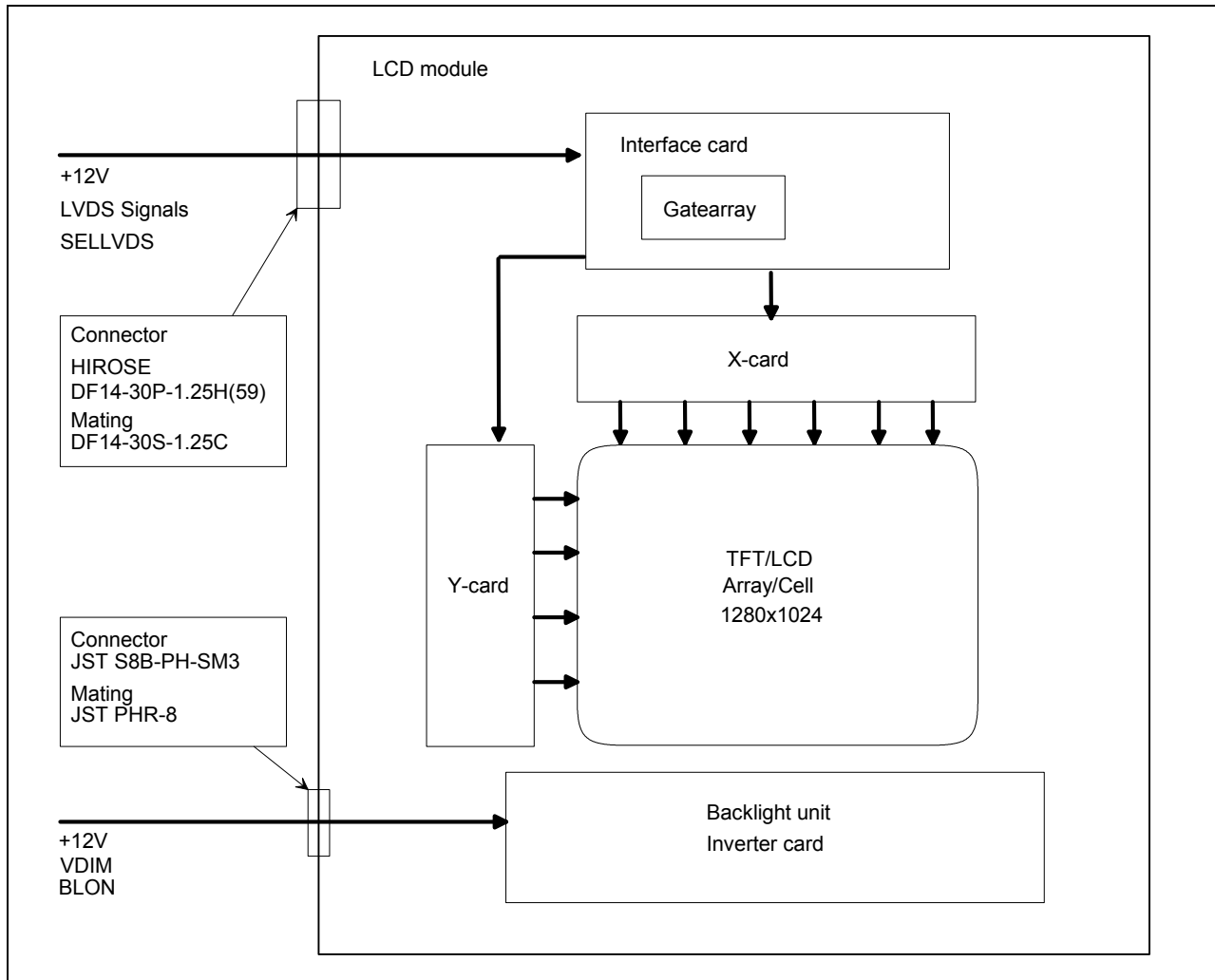
The following items are characteristics summary on the table under 25 degree C condition:

| CHARACTERISTICS ITEMS | SPECIFICATIONS |
|--------------------------------------|--|
| Screen Diagonal [mm] | 460 |
| Pixels H x V | 1280(x3) x 1024 |
| Active Area [mm] | 359.0(H) x 287.2(V) |
| Pixel Pitch [mm] | 0.2805(per one triad) x 0.2805 |
| Pixel Arrangement | Sub-pixel Vertical Stripe |
| Weight [grams] | 2,900 typ. |
| Physical Size [mm] | 389.0(W) typ. x 317.2(H) typ. x 35.0 (D) max. |
| Display Mode | Normally Black |
| Supported Grayscale | 8-bit per 1(one) sub-pixel |
| White Luminance [cd/m ²] | 700 Typ. |
| Contrast Ratio | 550 : 1 Typ. |
| Optical Rise Time/Fall Time [msec] | Rise Time + Fall Time : 40 Typ (total) |
| Input Voltage [V] | +12 +/- 5% |
| Power Consumption [W] | 38.8 typ., 46.6 max. |
| Electrical Interface | LVDS Dual (Even/Odd A/B/C Data(8bit), 3sync signals, Clock) |
| Temperature Range [degree C] | |
| Operating | 0 to +50 |
| Storage (Shipping) | -20 to +60 |

Note : Luminance : Rise / Fall Time:Respective 10% -> 90%, 90%->10%

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 18.1 Monochrome TFT/LCD Module.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

| Item | Symbol | Min | Max | Unit | Conditions |
|-------------------------|---------|------|------------|-------|-----------------------------------|
| Logic/LCD Drive Voltage | Vin | -0.3 | +13.2 | V | |
| Backlight Voltage | VBL | -0.3 | +13.2 | V | |
| Select LVDS data order | SELLVDS | -0.3 | 3.3 | V | |
| Brightness control | VDIM | -0.3 | 5.3 | V | |
| Backlight on signal | BLON | -0.3 | +5.3 | V | |
| Operating Temperature | TOP | 0 | +50 | deg.C | (Note 1) |
| Operating Humidity | HOP | 8 | 80 | %RH | (Note 1) |
| Storage Temperature | TST | -20 | +60 | deg.C | (Note 1) |
| Storage Humidity | HST | 5 | 95 | %RH | (Note 1) |
| Vibration | | | 1.5 10-200 | G Hz | (Note 2) |
| Shock | | | 50 11 | G ms | (Note 2) Half sine wave |

Note :

1. Maximum Wet-Bulb should be 39 degree C and No condensation.
 2. Vibration Specification
 - Sign Vibration:10-200-10Hz, 1.5G, 30 min, X, Y, Z Axis, Each One Time.
- Shock Specification
- Half sine wave:50G 11msec. -X+/-, -Y+/-, -Z+/- (Total 6 directions), Each one time Shock.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

| Item | Conditions | Specification | |
|--|--|---------------|--------------------|
| | | Typ. | Note |
| Viewing Angle (Degrees) K:Contrast Ratio | Horizontal (Right) K \geq 15 (Left) | 85 85 | - - |
| | Vertical (Upper) K \geq 15 (Lower) | 85 85 | - - |
| | Horizontal (Right) K \geq 10 (Left) | - - | 85 Min. 85 Min. |
| | Vertical (Upper) K \geq 10 (Lower) | - - | 85 Min. 85 Min. |
| Contrast ratio | | 550 | - |
| Response Time (ms) | Rising(10% \rightarrow 90%) + Falling(90% \rightarrow 10%) | 40 | - |
| White Balance | White x | 0.280 | - |
| | White y | 0.304 | - |
| Maximum White Luminance (cd/m ²) | VDIM=0V | 700 | - |

Note : Measure center of the screen.

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| | |
|------------------------------|--------------------|
| Connector Name / Designation | Signal Connector |
| Manufacturer | HIROSE |
| Type / Part Number | DF14-30P-1.25H(59) |
| Mating Type / Part Number | DF14-30S-1.25C |
| Contact / Part Number | DF14-2628SCFA |

| | |
|------------------------------|--|
| Connector Name / Designation | For Backlight Connector on Inverter card |
| Manufacturer | JST |
| Type / Part Number | S8B-PH-SM3 |
| Mating Type / Part Number | PHR-8 |

5.2 Interface Signal Connector

| Pin # | Signal Name | Pin # | Signal Name |
|-------|-------------|-------|-------------|
| 30 | Vin(+12V) | 29 | Vin(+12V) |
| 28 | Vin(+12V) | 27 | VinRTN(GND) |
| 26 | VinRTN(GND) | 25 | VinRTN(GND) |
| 24 | SELLVDS | 23 | (RESERVED) |
| 22 | DGND | 21 | RxOIN3+ |
| 20 | RxOIN3- | 19 | RxOCLKIN+ |
| 18 | RxOCLKIN- | 17 | RxOIN2+ |
| 16 | RxOIN2- | 15 | RxOIN1+ |
| 14 | RxOIN1- | 13 | RxOIN0+ |
| 12 | RxOIN0- | 11 | RxEIN3+ |
| 10 | RxEIN3- | 9 | RxECLKIN+ |
| 8 | RxECLKIN- | 7 | RxEIN2+ |
| 6 | RxEIN2- | 5 | RxEIN1+ |
| 4 | RxEIN1- | 3 | RxEIN0+ |
| 2 | RxEIN0- | 1 | LVDSGND |

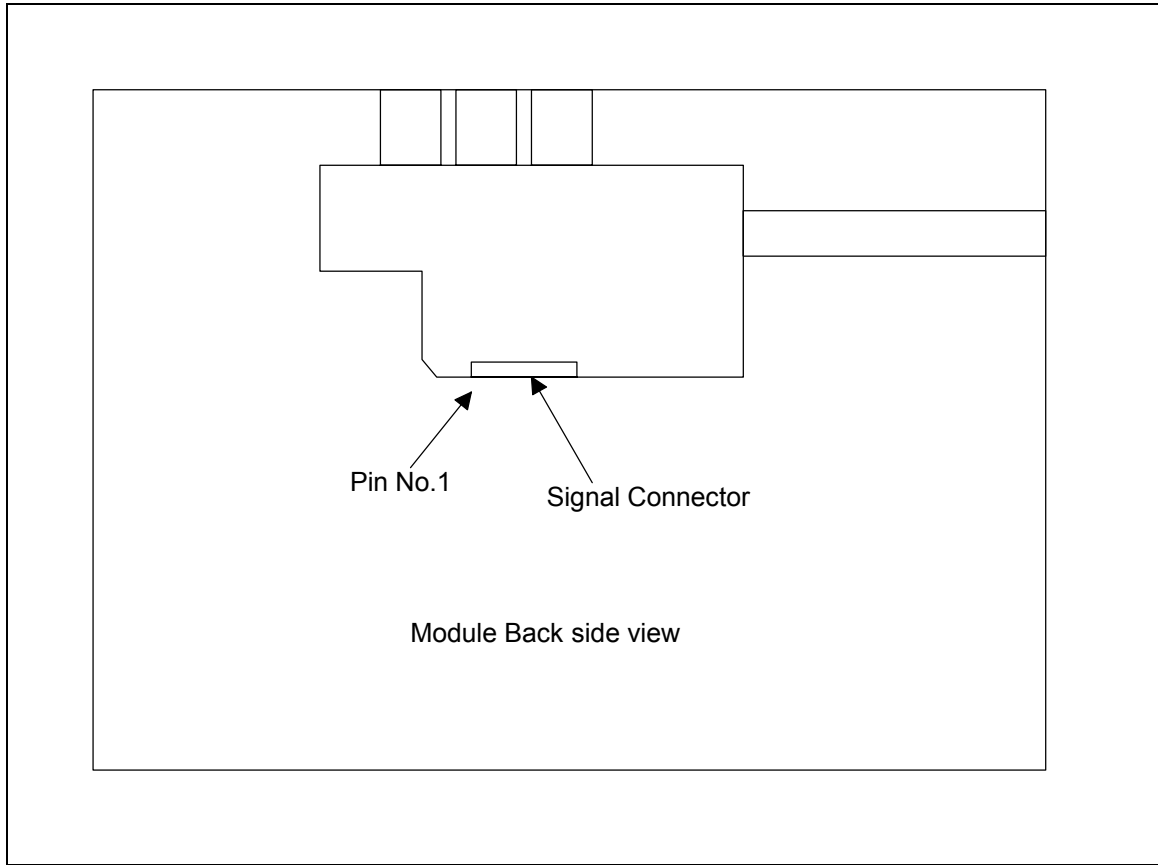
5.3 Interface Signal Description

The module uses a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible.

The first LVDS port (RxExxx) transmits even pixels while the second LVDS port (RxOxxx) transmits odd pixels.

Please refer to the chart below for pin #1 of Signal Connector.

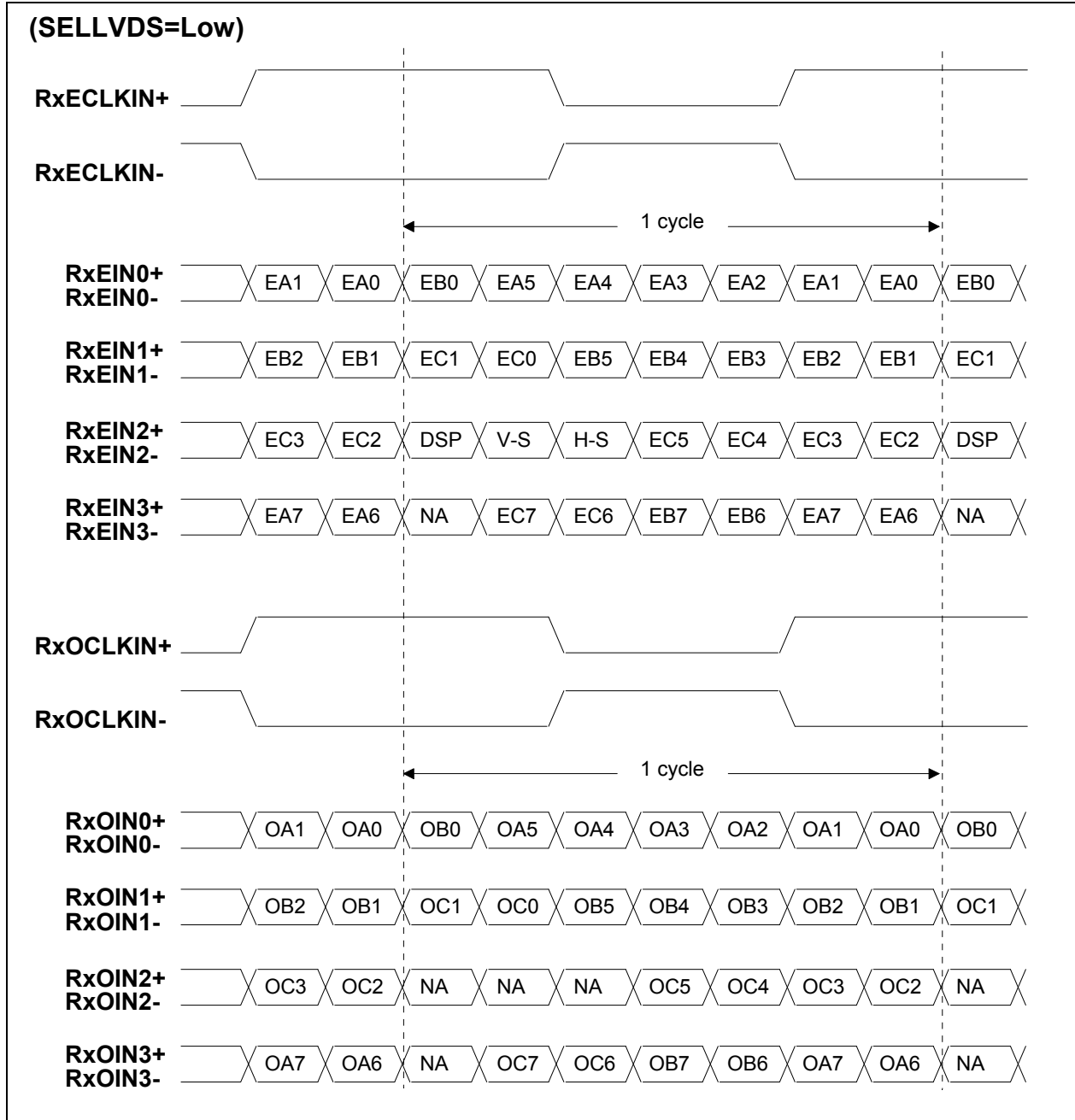
LCD Drive Connector No.1 Pin location



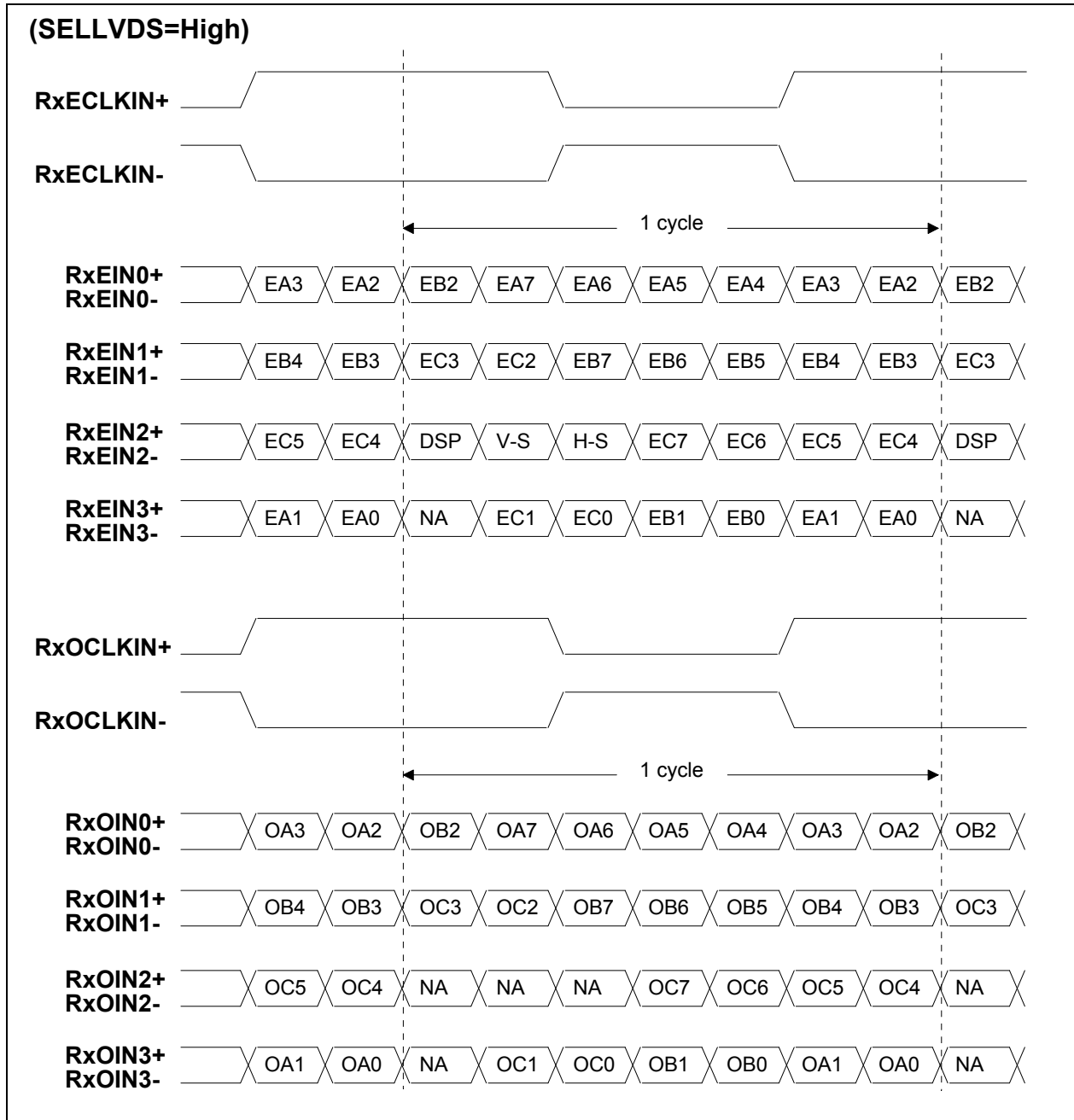
| PIN # | SIGNAL NAME | Description |
|-------|-------------|--|
| 30 | Vin | +12.0V Power Supply |
| 29 | Vin | +12.0V Power Supply |
| 28 | Vin | +12.0V Power Supply |
| 27 | VinRTN | Ground for Vin line |
| 26 | VinRTN | Ground for Vin line |
| 25 | VinRTN | Ground for Vin line |
| 24 | SELLVDS | Select LVDS data order. See the following figure. |
| 23 | (RESERVED) | This pin should be left open. |
| 22 | DGND | Signal Ground |
| 21 | RxOIN3+ | Positive LVDS differential data input (Odd data) |
| 20 | RxOIN3- | Negative LVDS differential data input (Odd data) |
| 19 | RxOCLKIN+ | Positive LVDS differential clock input (Odd Clock) |
| 18 | RxOCLKIN- | Negative LVDS differential clock input (Odd Clock) |
| 17 | RxOIN2+ | Positive LVDS differential data input (Odd data) |
| 16 | RxOIN2- | Negative LVDS differential data input (Odd data) |
| 15 | RxOIN1+ | Positive LVDS differential data input (Odd data) |
| 14 | RxOIN1- | Negative LVDS differential data input (Odd data) |
| 13 | RxOIN0+ | Positive LVDS differential data input (Odd data) |
| 12 | RxOIN0- | Negative LVDS differential data input (Odd data) |
| 11 | RxEIN3+ | Positive LVDS differential data input (Even data) |
| 10 | RxEIN3- | Negative LVDS differential data input (Even data) |
| 9 | RxECLKIN+ | Positive LVDS differential clock input (Even Clock) |
| 8 | RxECLKIN- | Negative LVDS differential clock input (Even Clock) |
| 7 | RxEIN2+ | Positive LVDS differential data input (Even data,H-Sync,V-Sync,DSPTMG) |
| 6 | RxEIN2- | Negative LVDS differential data input (Even data,H-Sync,V-Sync,DSPTMG) |
| 5 | RxEIN1+ | Positive LVDS differential data input (Even data) |
| 4 | RxEIN1- | Negative LVDS differential data input (Even data) |
| 3 | RxEIN0+ | Positive LVDS differential data input (Even data) |
| 2 | RxEIN0- | Negative LVDS differential data input (Even data) |
| 1 | DGND | Signal Ground |

Note: Input signals of odd and even clock shall be the same timing.

The interface card has a 100ohm resistor between positive and negative lines of each LVDS signal input on the internal circuit.



Note:A/B/C data 7:MSB, A/B/C data 0:LSB



Note:A/B/C data 7:MSB, A/B/C data 0:LSB

The following is LVDS Signal description.

| LVDS DATA NAME | Description |
|----------------|---|
| DSP | Display Timing When the signal is high, the pixel data shall be valid to be displayed. |
| V-S | Vertical Sync Both Positive and negative polarity are acceptable. |
| H-S | Horizontal Sync Both Positive and negative polarity are acceptable. |

| TI LVDS X'mitter (SN75LVDS83) Signal name | ITSX88E4 LVDS Signal (SELLVDS=Low) | ITSX88E4 LVDS Signal (SELLVDS=High) |
|---|---------------------------------------|--|
| D0 | A0 | A2 |
| D1 | A1 | A3 |
| D2 | A2 | A4 |
| D3 | A3 | A5 |
| D4 | A4 | A6 |
| D5 | A7 | A1 |
| D6 | A5 | A7 |
| D7 | B0 | B2 |
| D8 | B1 | B3 |
| D9 | B2 | B4 |
| D10 | B6 | B0 |
| D11 | B7 | B1 |
| D12 | B3 | B5 |
| D13 | B4 | B6 |
| D14 | B5 | B7 |
| D15 | C0 | C2 |
| D16 | C6 | C0 |
| D17 | C7 | C1 |
| D18 | C1 | C3 |
| D19 | C2 | C4 |
| D20 | C3 | C5 |
| D21 | C4 | C6 |
| D22 | C5 | C7 |
| D23 | NA | NA |
| D24 | H Sync | H Sync |
| D25 | V Sync | V Sync |
| D26 | Disp Timing | Disp Timing |
| D27 | A6 | A0 |

Note:

SELLVDS: Pin#7 of Signal connector

A0: LSB, A7: MSB

5.4 Interface Signal Electrical Characteristics

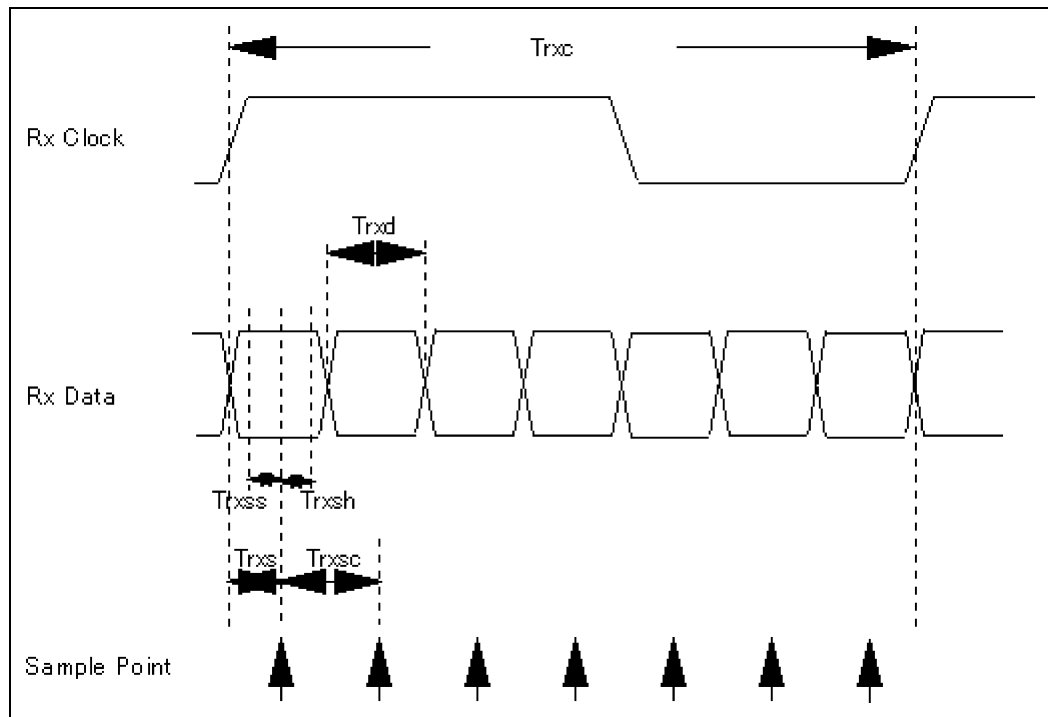
Input signals shall be low or Hi-Z state when V_{in} is off.

It is recommended to refer the specifications of SN75LVDS82DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

| Parameter | Condition | Min | Max | unit |
|-----------|---|------|-----|------|
| V_{th} | Differential Input High Voltage ($V_{cm}=+1.2V$) | | 100 | mV |
| V_{tl} | Differential Input High Voltage ($V_{cm}=+1.2V$) | -100 | | mV |

LVDS Timing



LVDS Macro AC characteristics.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------------|--------|------|---------|-----|------|
| LVDS Clock Cycle | Trxc | 17.6 | 18.5 | 20 | [ns] |
| LVDS Data Cycle | Trxd | | Trxc/7 | | [ns] |
| Sample Data Setup Time (Trxc=Typ.) | Trxss | 600 | | | [ps] |
| Sample Data Hold Time (Trxc=Typ.) | Trxsh | 600 | | | [ps] |
| Data Sample Time | Trxs | | Trxc/14 | | [ns] |
| Data Sample Cycle | Trxsc | | Trxc/7 | | [ns] |

| Name | Description | Min | Typ | Max | Unit | Note |
|---------|--------------|------|-----|-----|------|------|
| SELLVDS | High voltage | 2 | 3 | 3.3 | V | |
| | Low voltage | -0.1 | 0 | 0.7 | V | |
| | Current | -1 | - | 1 | mA | |

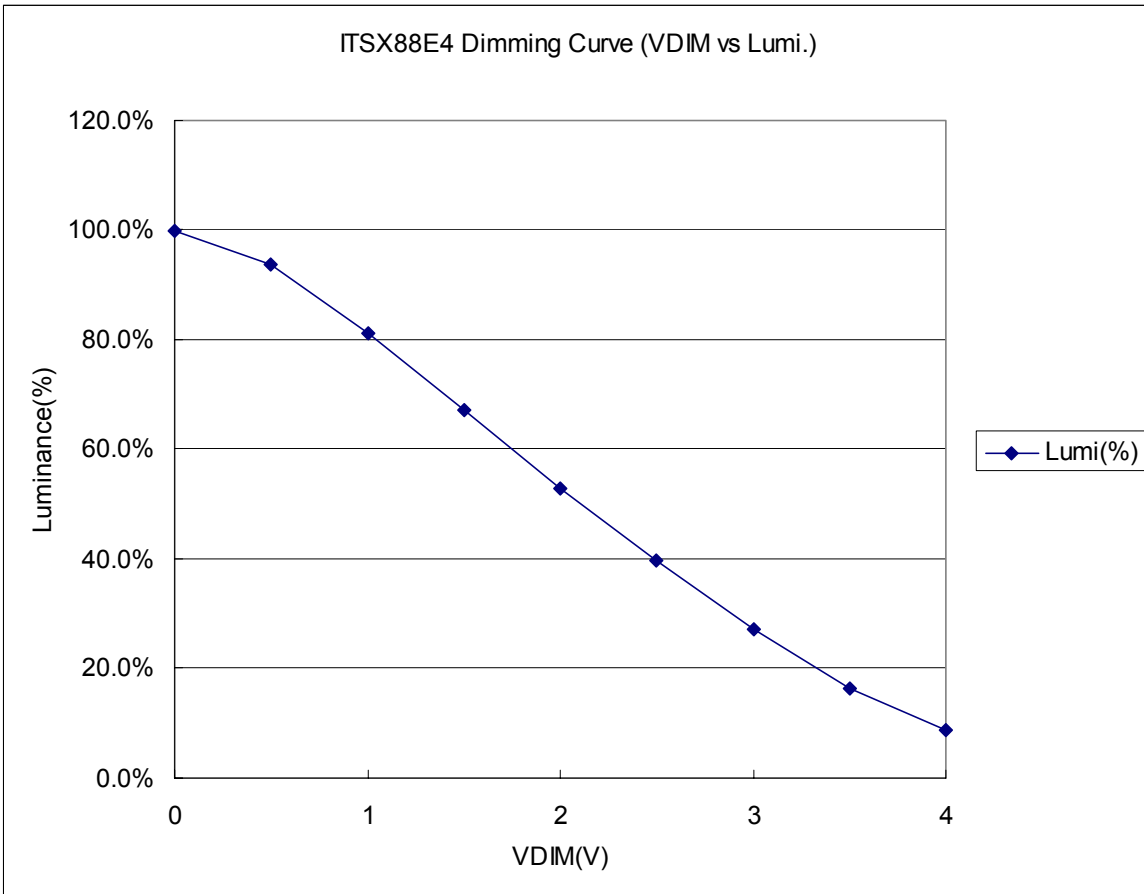
5.5 Backlight Connector Signal Description

| PIN # | SIGNAL NAME | Description |
|-------|-------------|--|
| 1 | VBL | +12.0V Power Supply for backlight |
| 2 | VBL | +12.0V Power Supply for backlight |
| 3 | VBL | +12.0V Power Supply for backliht |
| 4 | RTN | Ground for VBL line, VDIM and BLON |
| 5 | RTN | Ground for VBL line, VDIM and BLON |
| 6 | RTN | Ground for VBL line, VDIM and BLON |
| 7 | VDIM | Brightness control voltage input(0-4V), (0V:brightness MAX, 4V:brightness MIN) |
| 8 | BLON | backliht on/off signal(Hi:backlight ON, Low:backlight OFF) TTL level |

5.6 Backlight Input Signal Electrical Characteristics

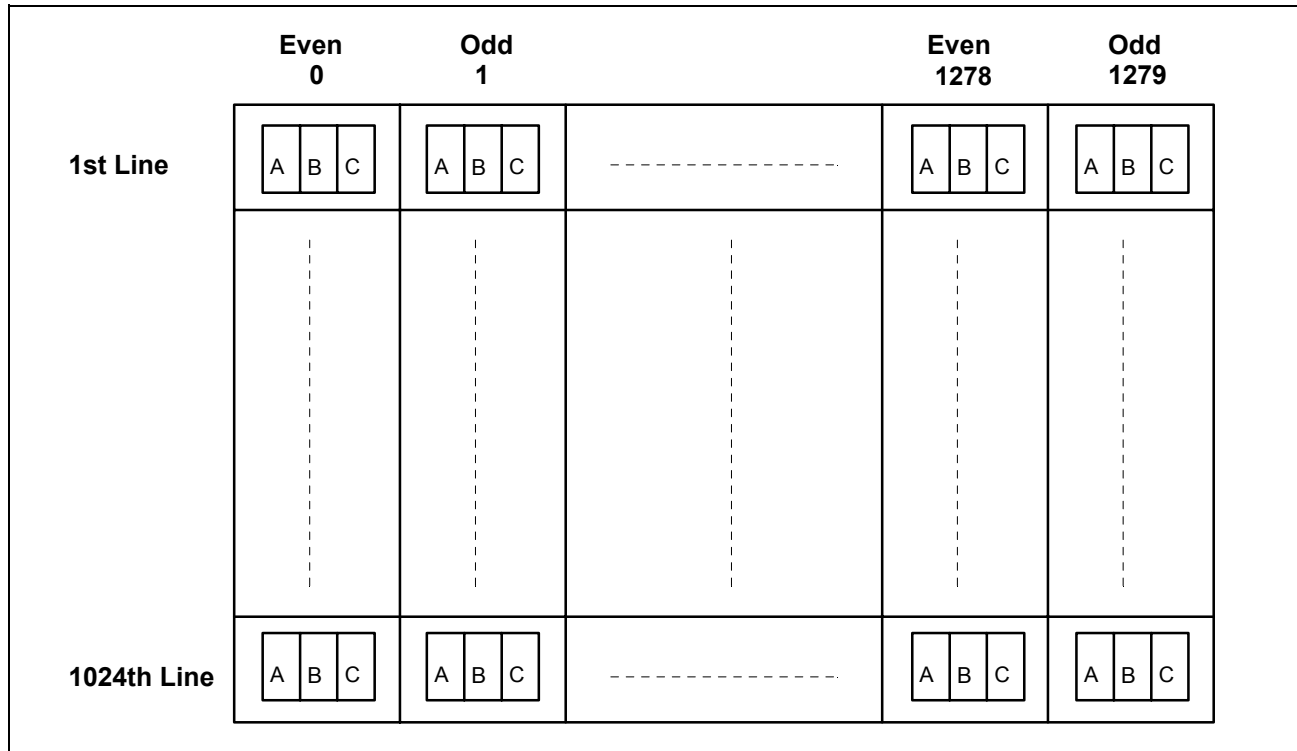
| Name | Description | Min | Typ | Max | Unit | Note |
|------|---------------------|------|-----|------|------|--|
| BLON | High voltage | 2.0 | 5.0 | 5.25 | V | |
| | Low voltage | -0.1 | 0 | 0.8 | V | |
| | Current | -1.0 | - | 1.0 | mA | |
| VDIM | Input Voltage Range | 0 | - | 4.0 | V | 0V: Brightness Max. 4V: Brightness Min. |
| | Current | -1.0 | - | 1.0 | mA | |

The following chart is the Dimming Signal (VDIM) versus Luminance curve for your reference.



6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Odd and even pair of ABC data are sampled at a time.



7.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS82DGG(Texas Instruments) or equivalent.

7.1 Timing Characteristics

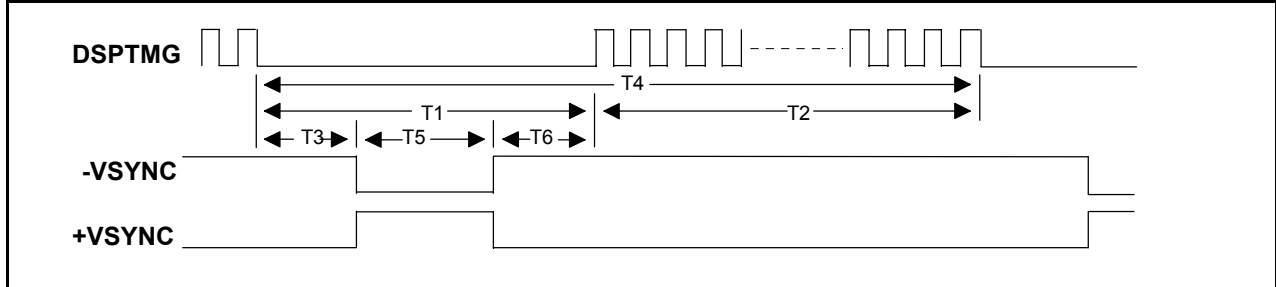
| Signal | Item | Symbol | MIN. | TYP. | MAX. | Unit |
|---------|----------------|---------|-------|-------|-------|-------|
| DTCLK | Freq. | Fdck | 50 | 54 | 56.8 | MHz |
| DTCLK | Cycle | Tck | 17.6 | 18.5 | 20 | ns |
| +V-Sync | Frame Rate | 1/Tv | 56.25 | 60.02 | 61 | Hz |
| +V-Sync | Cycle | Tv | 16.39 | 16.66 | 17.78 | ms |
| +V-Sync | Cycle | Tv | 1035 | 1066 | 2047 | lines |
| +V-Sync | active level | Tva | 3 | 3 | | lines |
| +V-Sync | V-back porch | Tvb | 7 | 38 | 63 | lines |
| +V-Sync | V-front porch | Tvf | 1 | 1 | | lines |
| +DSPTMG | V-Line | m | - | 1024 | - | lines |
| +H-Sync | Scan Rate | 1/Th | - | 63.98 | - | KHz |
| +H-Sync | Cycle | Th | 844 | 844 | 1023 | Tck |
| +H-Sync | active level | Tha(*1) | 4 | 56 | | Tck |
| +H-Sync | Back porch | Thb(*1) | 4 | 124 | | Tck |
| +H-Sync | Front porch | Thf | 4 | 24 | | Tck |
| +DSPTMG | Display Pixels | n | - | 640 | - | Tck |

Note :

- Typical value is refer to VESA STANDARD.
(*1): Tha+Thb should be less than 1024 Tck.
- When there are invalid timing, Display appears black pattern.
Synchronous Signal Defects and enter Auto Refresh for LCD Module Protection Mode.

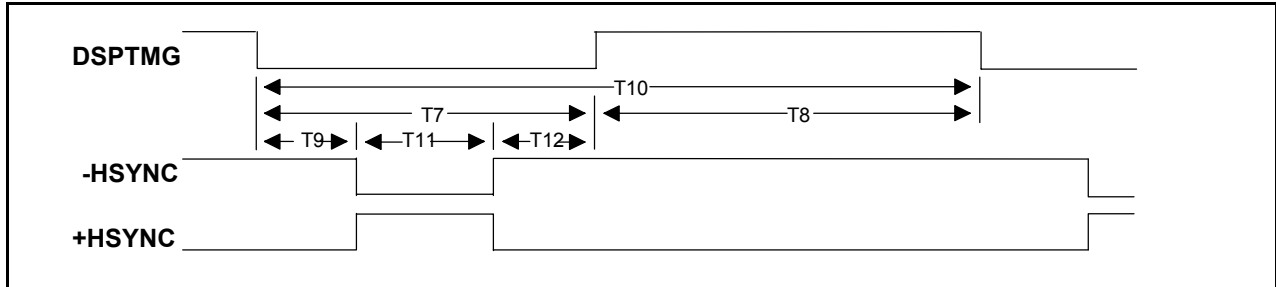
7.2 Timing Definition

Vertical Timing



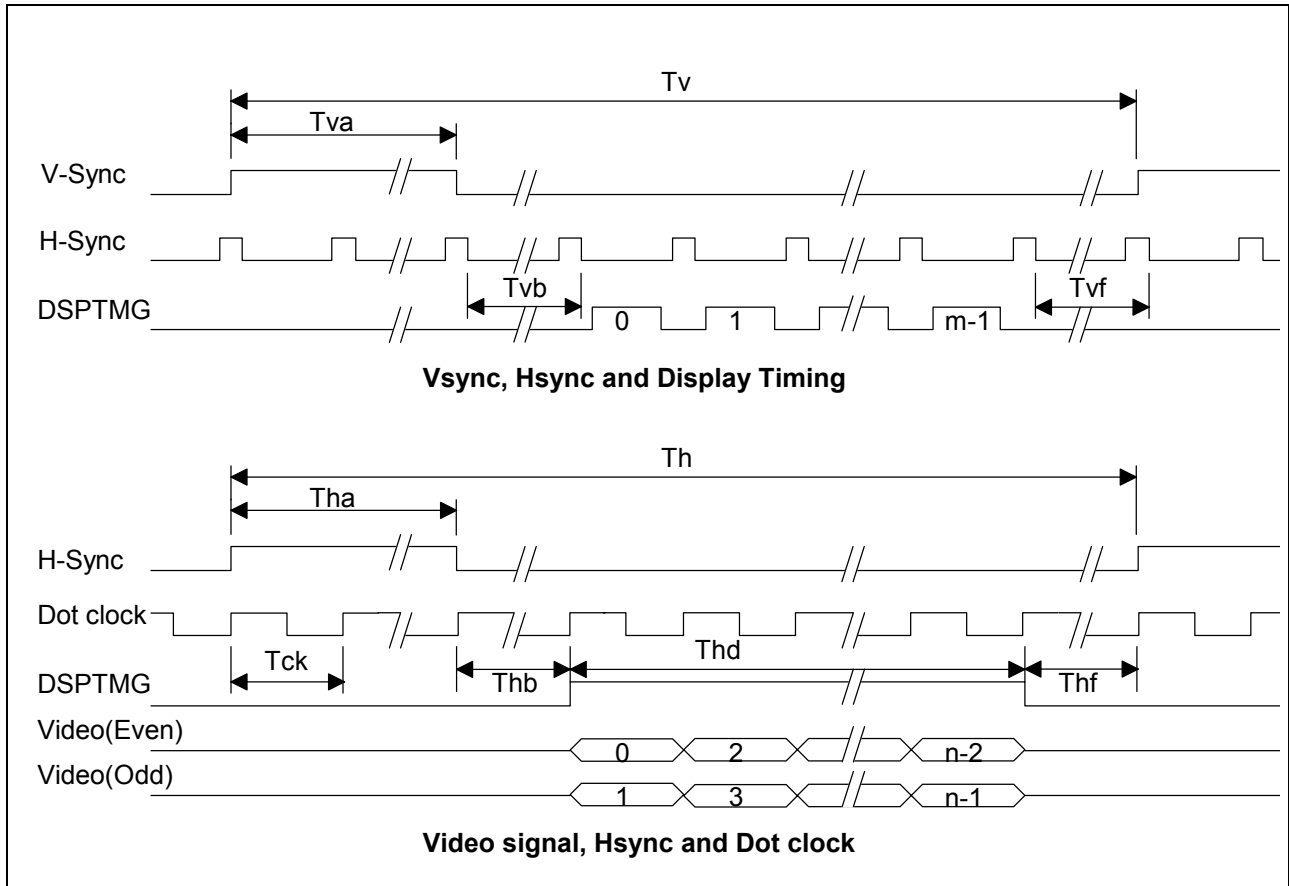
| Support mode | T1 Vertical Blanking | T2 Active Field | T3 VSYNC Front Porch | T4 Frame Time | T5 VSYNC Width | T6 VSYNC Back Porch |
|---|------------------------|---------------------------|----------------------|---------------------------|-----------------------|------------------------|
| 1280 x 1024 at 60Hz (VESA STANDARD) (H line rate : 15.6 us) | 0.656 ms (42 lines) | 16.005 ms (1024 lines) | 0.016 ms (1 line) | 16.661 ms (1066 lines) | 0.047 ms (3 lines) | 0.594 ms (38 lines) |

Horizontal Timing



| Support mode | T7 Horizontal Blanking | T8 Active Field | T9 HSYNC Front Porch | T10 H line Time | T11 HSYNC Width | T12 HSYNC Back Porch |
|--|------------------------|--------------------------|-----------------------|--------------------------|------------------------|------------------------|
| 1280 x 1024 (VESA STANDARD) (Dotclock : 108.000 MHz) | 3.778 us (408 dots) | 11.852 us (1280 dots) | 0.444 us (48 dots) | 15.630 us (1688 dots) | 1.037 us (112 dots) | 2.296 us (248 dots) |

Interface Timing Definition



8.0 Power Consumption

Input power specifications are as follows;

| SYMBOL | PARAMETER | Min | Typ | Max | UNITS | CONDITION |
|--------|--|--|------|------|-------|--|
| Vin | Logic/LCD Drive Voltage | 11.4 | 12 | 12.6 | V | |
| Iin | Vin Current | | | 550 | mA | All White Pattern Vin=11.4V (*1) |
| Pin(1) | Vin Power | | 4.5 | | W | Typical Load Condition (Vertical Gray Bar, 256 Scale) |
| Pin(2) | | | 5.2 | 6.3 | W | Maximum Load Condition (All White) |
| | Logic/LCD DC current Waveform | Refer to the Typical Logic/LCD Current Waveform shown in the following Figure. Waveform may vary in particular application. Actual current waveform on user application must be evaluated and make sure the ripple current and/or peak current should be allowable to user power supply. | | | | Maximum Load Condition (All White) |
| Vin rp | Allowable Logic/LCD Drive Ripple Voltage | | | 500 | mVp-p | |
| VBL | Backlight power voltage | 11.4 | 12 | 12.6 | V | |
| PBL | Backlight power consumption | | 33.6 | 40.3 | W | Brightness = max. |

Note : A used DC power supply for this LCD module should be have a over current protection function to safety.

(*1) This value indicates long term average.

Typical Logic/LCD Current Waveform

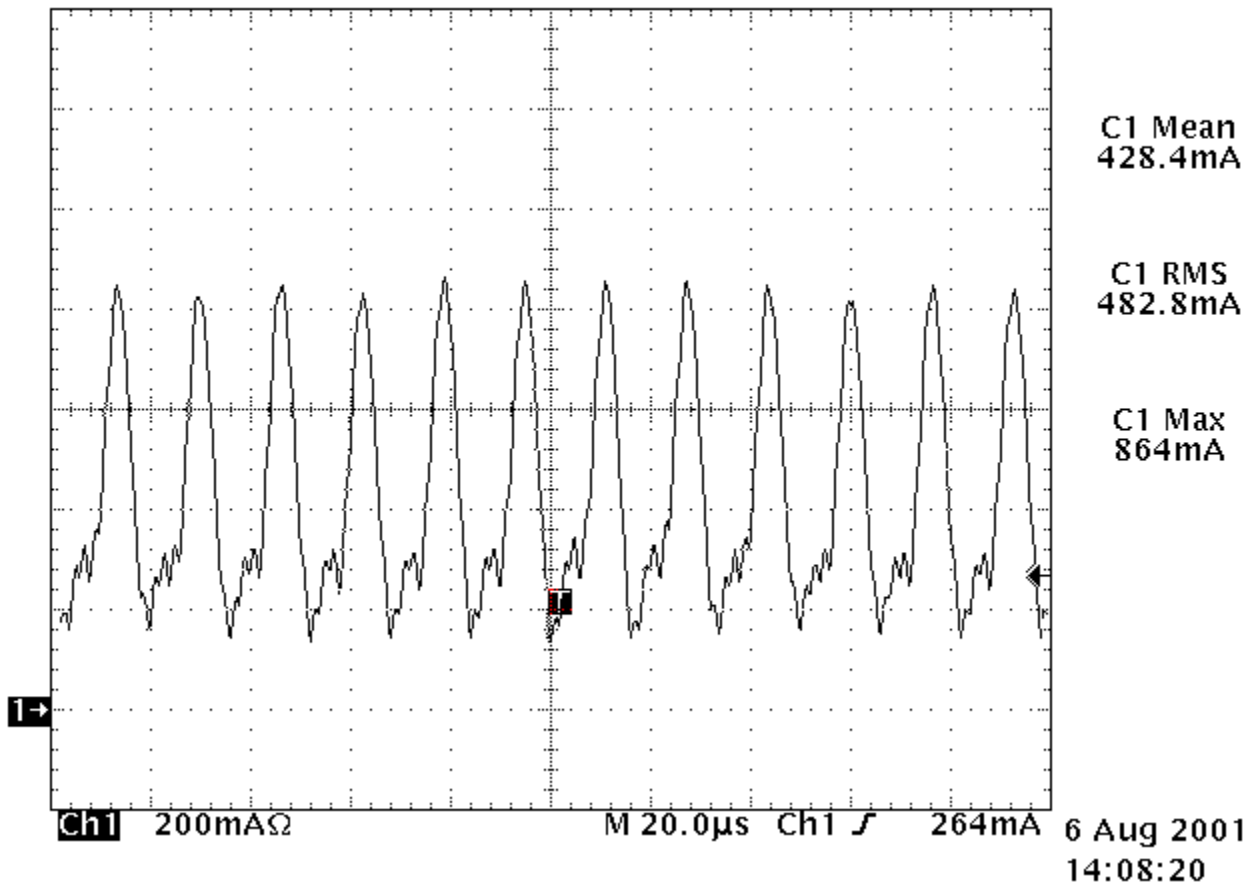
Condition : Maximum Load Condition(All White)

Voltage : 12.0V measured at Interface Connector J1

Interface Cable : AWG28, 30 Conductors, L=500mm from Voltage Source to EUT

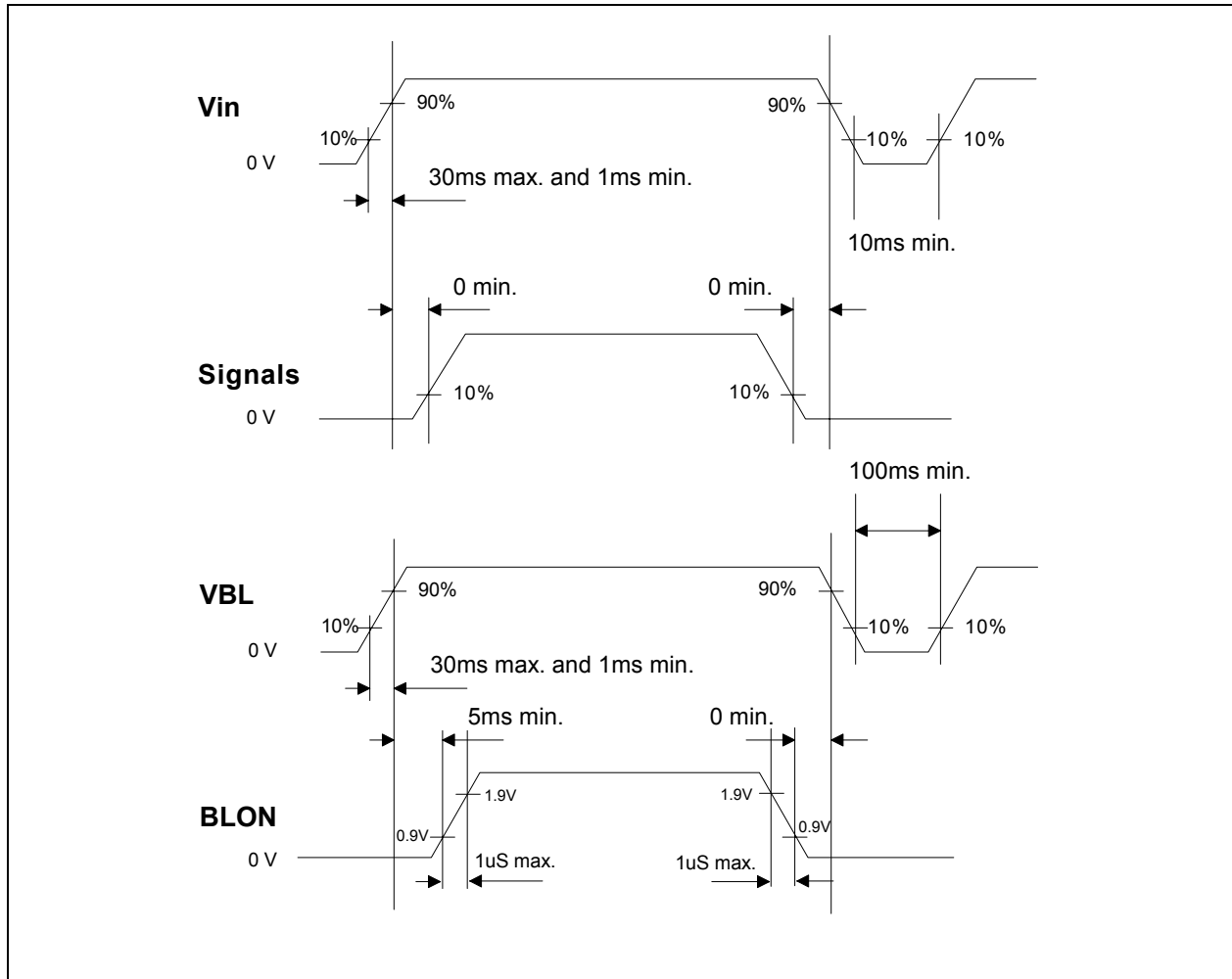
Tek Stop: 2.50MS/s

42 Acqs



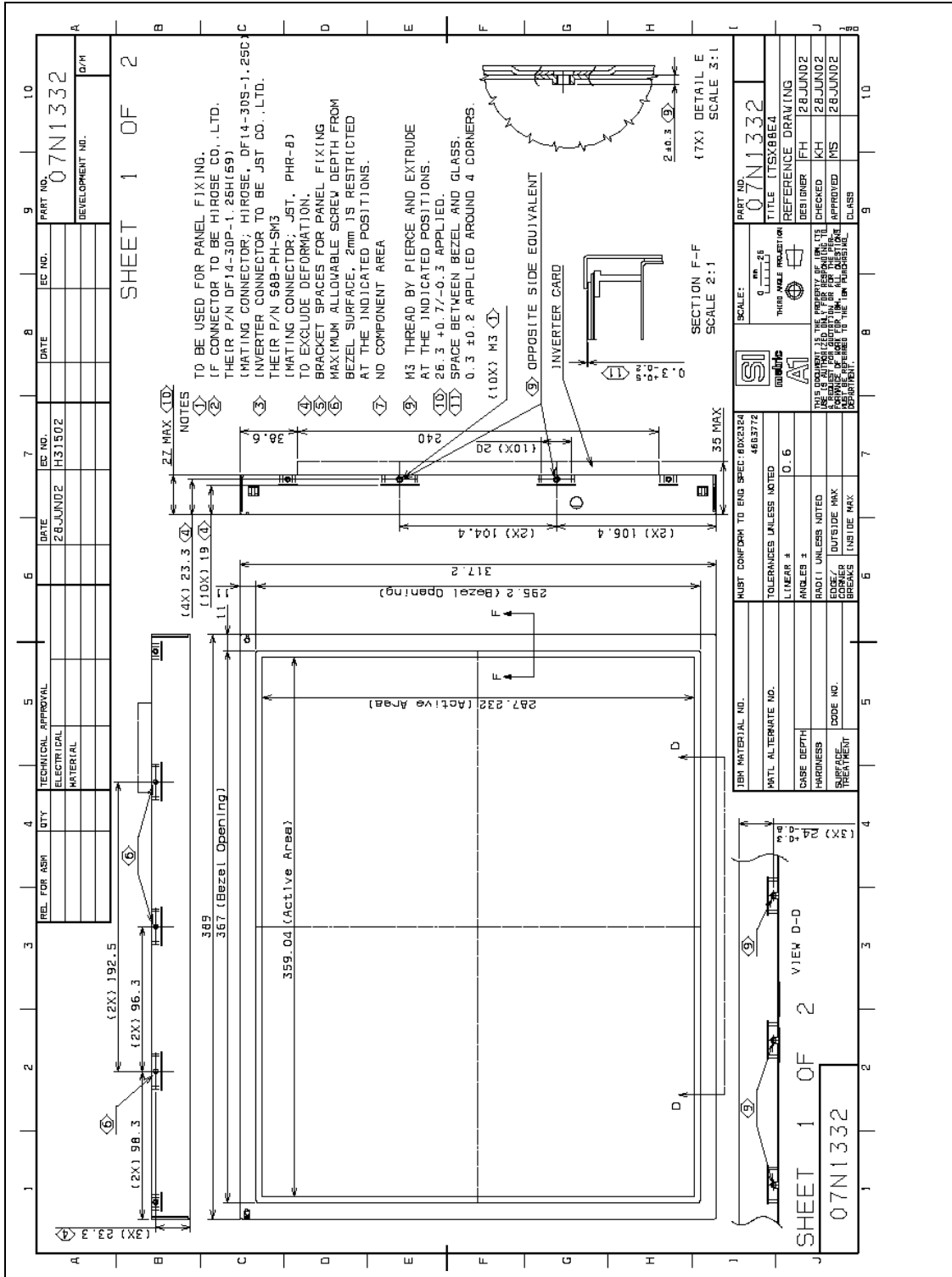
9.0 Power ON/OFF Sequence

Vin and VBL power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when Vin and VBL are off. It is recommended that the BLON should be supplied after other signals are stable in order to avoid visible screen noise when power-on.



10.0 Mechanical Characteristics

Note : Please do not use middle 3(three) screw holes on the upper(long) side and middle 3(three) screw holes on the lower(long) side for panel fixing. These screw holes are for manufacturing purpose only.



11.0 National Test Lab Requirement

The display module will satisfy all requirements for compliance to
UL60950 3rd. Ed. U.S.A. Information Technology Equipment

***** End Of Page *****